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Broadband, low-loss O-band Silicon Polarization Splitter-Rotator

(Student paper)

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A novel O-band polarization splitter-rotator based on mode conversion and coupling is proposed. The device is broadband, tolerant to fabrication imperfections and compatible with DUV lithography MPW processes, requiring single-step etching. Simulations show $TM_0 \rightarrow TE_0$ efficiency greater than 89% across the O-band with peak value of 96.3%, and TE_0-TE_0 efficiency of >99%. The simulated crosstalk is <-85 dB and the polarization dependent loss <0.5 dB in the O-band.
Keywords: *Silicon Photonics, polarization splitter-rotator, O-band*

INTRODUCTION

Silicon Photonics (SiPh) technology has gained attention in recent years, due to its compatibility with CMOS fabrication processes [1] that enable the low-cost development of photonic integrated circuits (PIC) with sub-micron precision, through multi-project wafer (MPW) services [2]. The high index contrast of the material allows the development of ultra-compact devices that can also be low-power and tightly co-integrated with electronics. However, silicon-on-insulator (SOI) waveguides exhibit strong birefringence which makes the SiPh devices highly polarization-sensitive. To overcome this drawback different approaches have been exploited to achieve on-chip polarization diversity [3]. Polarization splitters-rotators (PSR) are key components in polarization diversity circuits, necessary at the interface between fibers and PICs. They are also important in various applications, like coherent optical receivers, data-centre transceivers and quantum photonics [4]. However, it is difficult to realize waveguide-type polarization rotators since it is complicated to rotate the optical axis of a planar waveguide. To achieve that, the symmetry of the waveguide cross-section must be broken [5]. Different types of PSRs have been reported employing cascaded bends, stacked waveguides, bi-level tapers, off-axis dual cores, subwavelength structures and slanted waveguides [6]–[8]. These structures, although they usually show good performance, require complex fabrication processes like multiple etch-depths and special etching and have low fabrication tolerance. Moreover, very few O-band PSRs that meet the requirements for easy fabrication and tolerance have been proposed.

In this work, we propose a broadband O-band PSR based on mode conversion and phase matching that implements the TM_0-TE_1-TE_0 mode conversion in a structure that consists of an adiabatic taper and an asymmetric directional coupler (ADC) with one tapered arm [9]. Air is used as top cladding to break the vertical symmetry, therefore only a single etch depth is necessary, making its fabrication simple and fully compatible with deep-UV lithography MPW processes [10]. The tapered ADC improves its tolerance to fabrication imperfections. The PSR is compatible with the 100G CWDM4 MSA Ethernet standard. In this paper, we describe the detailed simulation and design process of the PSR and report its simulated performance.

SIMULATIONS AND DESIGN

The proposed PSR is designed on a 220 nm SOI wafer and the refractive indices for Si and SiO_2 are n_{Si} = 3.504 and n_{SiO2} = 1.4469 at 1300 nm respectively. As shown in Fig. 1 Left, the device consists of two sections, the taper and the coupler, connected to the input and output waveguides with nominal widths (w_0=w_{out}=380 nm). The principle of operation of the PSR is based on mode conversion ($TM_0 \rightarrow TE_1$) in the taper and mode coupling due to phase matching ($TE_1 \rightarrow TE_{0\text{-cross}}$) in the coupler. The TE_0 at the input propagates unchanged through the PSR to the through port, while TM_0 is rotated to TE_0 at the cross port.

Fig. 1 Right shows the effective indices (n_{eff}) of the eigenmodes of the Si waveguide varying its width, as calculated using the Finite Difference Eigenmode (FDE) solver by Lumerical. Due to the vertical asymmetry introduced by the air top-cladding, for a critical width of around 590 nm, the TM_0-TE_1 modes are hybridized and therefore mode conversion is achieved around this region. The taper widths are selected so that the taper input (w_0) is single mode, while its output (w_3) also supports mode TE_1. As w_0 the nominal waveguide width is selected (w_0=380 nm). w_3 is selected to be larger than the critical width so that the whole hybridization region is included in the taper (w_3=750 nm). To achieve adiabatic mode conversion with high efficiency and short length, a three-segment taper approach is employed. The middle segment (L_{tp2}) is where the mode conversion happens. It should include the

critical width for all operation wavelengths and should have a very small taper angle to be adiabatic. The first and third segments (L_{tp1}, L_{tp3}) can have steeper slopes to ensure a short taper, without compromising the efficiency. We choose w_1=500 nm and w_2=670 nm (w_1<590 nm<w_2).

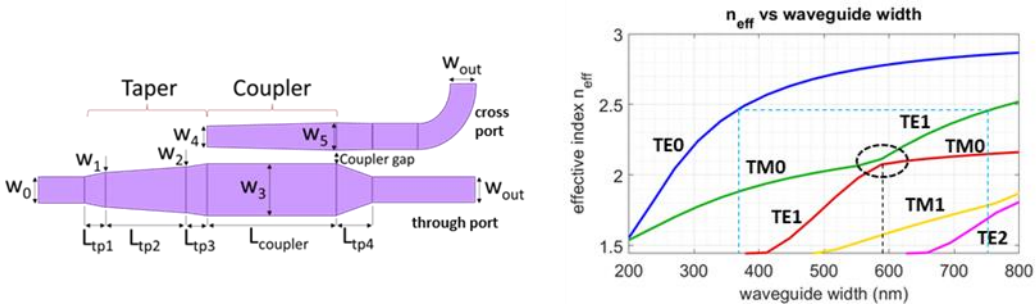

Fig. 1: Left: Top view of the geometry of the proposed PSR. Right: the calculated effective indices of the eigenmodes of a Si waveguide with air top-cladding and Si height of 220 nm vs. the waveguide width.

The lengths of the three segments are optimized with the EigenMode Expansion (EME) propagation solver by Lumerical, to achieve maximum mode conversion efficiency (MCE) at 1300 nm. Fig. 2 (a) shows the TE_0-TE_0 and TM_0-TE_1 efficiency varying the middle segment length. The optimal length is calculated to be L_{tp2}=170 μm, where $MCE_{TM0\text{-}TE1}$ = 97%. We also calculate L_{tp1}=7 μm and L_{tp3}=11 μm. No coupling occurs for TE_0 in this region, therefore TE_0 propagates unchanged through the taper with efficiency of almost 100%.

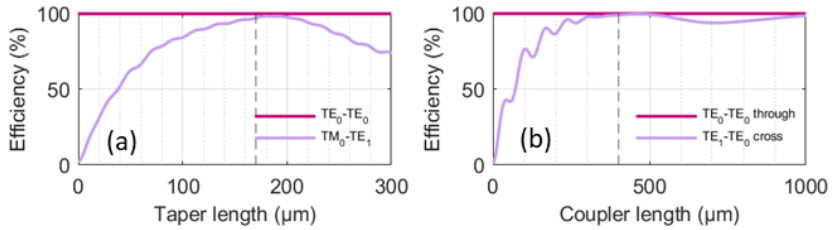

Fig. 2: (a) MCE of TM_0-TE_1 and TE_0-TE_0 propagation vs. length of the taper section L_{tp2}, (b) MCE of TM_0-TE_1 and TE_0-TE_0 propagation vs. coupler length $L_{coupler}$.

After converting TM_0 to TE_1, a narrow, tapered waveguide is placed next to the wide waveguide at the output of the taper section, to form an ADC. With correct choice of the waveguide widths of the ADC, the phase matching condition is satisfied, meaning n_{eff_TE1} at the wide waveguide is equal to n_{eff_TE0} at the narrow one. This way, TE_1 will be efficiently coupled to TE_0 at the cross waveguide. For w_3=750 nm, this is satisfied for a width of around 365 nm for the narrow waveguide (highlighted in Fig. 1 Right with dashed light blue lines). In the case of a cross waveguide with uniform width, the latter would have to be chosen with nanometer accuracy and any deviation induced by fabrication would cause the breaking of the phase matching condition. By making it tapered, the fabrication tolerance of the design is improved, since even if the final dimensions deviate from the specified ones, the phase matching condition will be met at some point along the taper. Also, the bandwidth of the design is enlarged, since the phase matching points are slightly different for the various O-band wavelengths, but they can always be found along the coupling region. Eventually, we choose w_4=340 nm and w_5=390 nm (around the 365 nm phase matching point for 1300 nm). Also, the coupler gap is chosen to be ≥180 nm ensuring low fabrication complexity. Then, the length of the coupler is optimized using the EME solver to maximize the coupling efficiency. The simulation results are shown in Fig. 2 (b). The optimal length is found to be $L_{coupler}$=400 μm wielding a TE_1-$TE_{0\text{-cross}}$ efficiency of 99% at 1300 nm. For the TE_0 at the wide waveguide in the coupling section, no phase matching condition is satisfied, so TE_0 will propagate straight to the through port with very small crosstalk at the cross port and negligible losses.

Fig. 3 shows the simulated light propagation across the whole device, generated using the EME solver. For TE_0 input (Fig. 3(a)) all the power propagates to the through port, while for TM_0 input (Fig. 3(b)), it is rotated to TE_1 and then coupled to TE_0 of the cross output port. The transmission and crosstalk varying the wavelength across the O-band

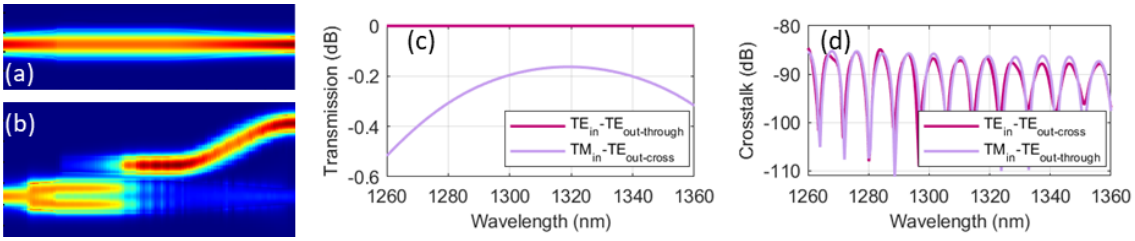

Fig. 3: (a) Top view of the simulated light propagation along the PSR with TE_0 input mode and (b) TM_0 input mode. (c) Simulated wavelength characteristics of the proposed PSR. The TE_0-TE_0 and TM_0-TE_0 transmissions. (d) The crosstalk.

are shown in Fig. 3 (c) and (d) respectively. The TE_{in}-$TE_{out\text{-}through}$ insertion loss is almost 0 dB across the O-band, while the TM_{in}-$TE_{out\text{-}cross}$ conversion loss is <0.5 dB, making the design highly efficient and broadband. The crosstalk for both TE and TM input is <-85 dB across the O-band. The polarization dependent loss (PDL) is <0.5 dB in the O-band.

Since this is an on-chip PSR that will be connected at its input and output with standard waveguides with SiO_2 top-cladding, the EME solver was used to simulate the interface. It was thus verified that no losses are introduced because of the different cladding, and coupling efficiency is almost 100% for both propagation directions.

A tolerance study was carried out to investigate the effect of the variation of two parameters on the PSR performance: the waveguide width (Δw), induced by variations of the lithography process, and of the SOI wafer height (Δh). Typically, Δw is limited to ±5 nm for DUV lithography and Δh to ±2 nm, however we varied them in a wider range for certainty [11]. The results are reported in Fig. 4 (a) and (b) respectively. Polarization conversion loss for TM_0 input remains below 0.5 dB for Δw = ±10 nm and below 1.5 dB for Δh = ±5 nm. This showcases a very good tolerance to fabrication imperfections and full compatibility with MPW services. This is very important for real applications that require reliable, efficient and broadband PSRs, without having access to more advanced and expensive fabrication techniques. In this regard, the design has been included in an MPW chip submission (under fabrication), targeting the development of SiPh coarse wavelength division multiplexing (CWDM) transceivers for High Energy Physics (HEP) experiments at CERN [12], that require on-chip polarization diversity.

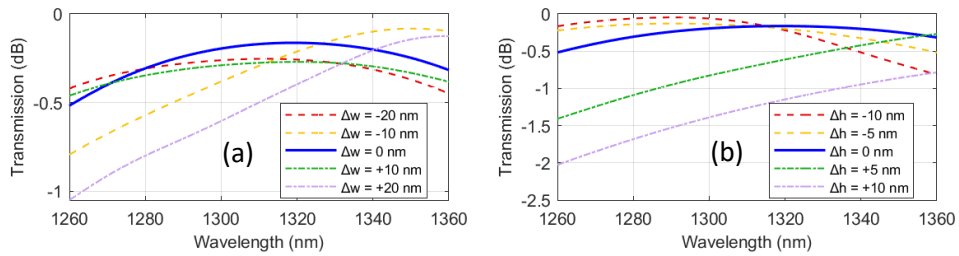

Fig. 4: TM_{0in}-$TE_{0cross\text{-}out}$ transmission varying (a) the width of the PSR and (b) the height of the SOI wafer.

CONCLUSIONS

We presented a novel broadband PSR element designed for the 220-nm top SOI integration platform. The design has a length of 610 μm. Simulations show a TE-TE efficiency of >99% across the O-band, and TM-TE MCE of 96% at 1310 nm and >89% across the O-band. The simulated PDL is <0.5 dB across the O-band and <0.4 dB in the 100G CWDM grid. The crosstalk is <-85 dB in the O-band. The novelty of the design is built upon a mode hybridization taper and tapered ADC for the mode coupling, resulting in low complexity fabrication, low loss and broadband O-band operation, while showcasing increased tolerance to fabrication imperfections. It employs a single etch depth and is fully compatible with deep UV lithography MPW processes. It has been included in an MPW chip submission as part of a SiPh test chip for HEP experiments at CERN.

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