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Electro-Optic Packaging of Silicon Photonics-Based RF Multiplier for Clock Signal Generation in the Millimeter-Wave Band

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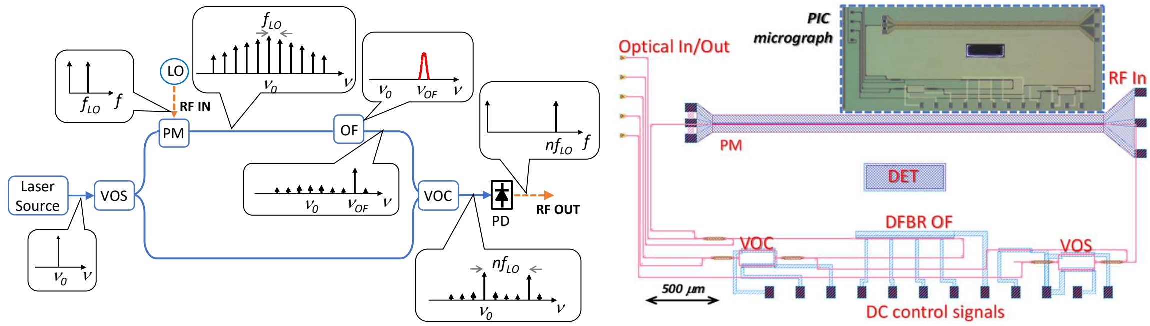
The design stages of a packaged silicon photonics RF processor for mm-wave reference clock distribution in 5G/6G radio access networks are presented. A wideband interconnection board including high-power handling bias tee is designed and implemented. Preliminary on-chip validation confirms spectrally pure 100 GHz signal generation from a 20 GHz input tone.
Keywords: *Integrated microwave photonics, silicon photonics, opto-electronic packaging*

INTRODUCTION

In 5G/6G mobile networks, operations such as ultra-low latency communications or wireless backhauling can be supported through high-capacity wireless links in the millimeter (mm)-wave band, where large bandwidth is available [1]. The quality of the radio signal would benefit from distributing a reference clock from a centralized base station toward network's peripherals using radio-over-fiber (RoF) approaches. By overcoming the impairments associated with recovering local clocks from jittered data samples, a common time reference enforces coordinated operations such as carrier aggregation or joint MIMO transmission techniques [2]. Additionally, costly RF oscillators at the antenna sites can be avoided, which is an appealing feature in the dense-cell architecture of 5G/6G networks. A further reduction of the system costs can be introduced by developing suitable photonic-integrated RF frequency synthetisers, and we recently demonstrated on-chip sixfold frequency multiplication of a microwave source up to 110 GHz with negligeable excess phase noise (PN) in a photonic integrated circuit (PIC) realized in silicon-on-insulator (SOI) technology [3]. Careful interfacing with the driving electronics and compact electro-optic packaging is however required for evaluating the circuit performance in field trials and its subsequent deployment in practical application scenarios. The design strategy for a miniaturized functionally packaged silicon photonics (SiP)-based programmable RF frequency multiplier is here reported. A matching network for the RF signal feeding the PIC is designed for operating over a wide frequency range of $\sim$8 GHz centered around 20 GHz, and subsequently implemented on a printed circuit board (PCB). The design also aims at providing large tolerance to load conditions for the on-chip SiP electro-optic modulator as well as to the variations in the length of the wedge-bonds required for board-to-PIC connection. Preliminary on-chip characterization of the circuit operation is reported.

CIRCUIT OPERATION AND IMPLEMENTATION

The operation of the photonic-integrated RF synthesizer is illustrated in Fig. 1(a), where the RF/optical signals spectra along the circuit are also schematized in the insets. An external laser source (LS) delivers an optical carrier at the optical frequency ν_0 to the PIC. The circuit then relies on optical frequency comb (OFC) generation in a carrier-depletion-based SiP phase modulator (PM) driven by a local oscillator (LO) signal at f_{LO} followed by a highly selective bandpass optical filter (OF) that isolates a single tone out of the comb and suppresses all the other spectral components. The output of the filter is then recoupled with the input laser carrier portion that is obtained by splitting the PIC input signal. The circuit output thus consists of an optical carrier and a single high-order harmonic sideband spaced by nf_{LO} from ν_0, being n the selected harmonic order. This signal is thus suitable for being transmitted over a RoF link without suffering from the RF power fading effect associated with the interplay of fiber chromatic dispersion and symmetric spectrum of standard dual-sideband modulation. The on-chip input variable optical splitter (VOS) and output variable optical coupler (VOC) allow the relative carrier-to-sideband amplitude levels to be precisely controlled at the PIC output for optimizing the RF output power generated by a high-speed photodiode (PD) after a fiber link. The mask layout used for circuit realization through a standard multi-process wafer service in SOI technology [4] is then shown in Fig. 1(b), along with a micrograph of the fabricated device. The



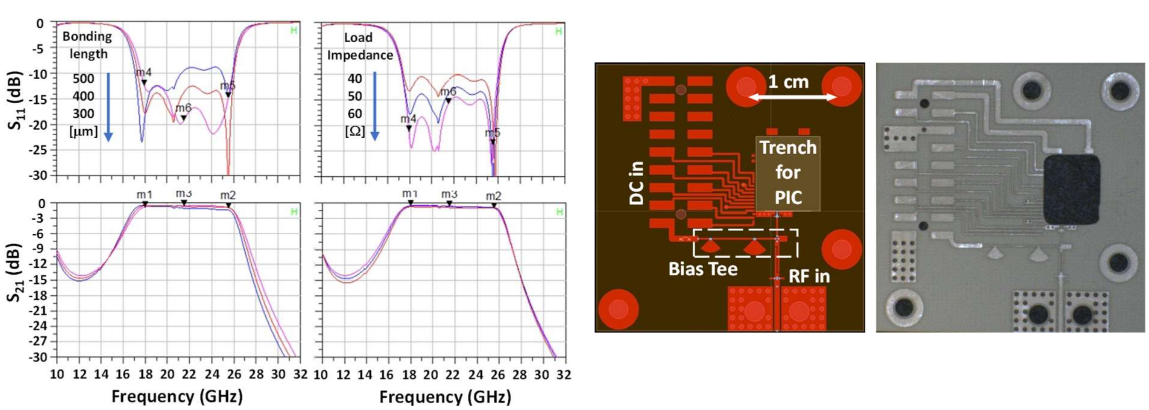
(a) (b)

Fig. 1. (a) Operation scheme; (b) Mask layout for circuit implementation in SOI technology (inset: micrograph of fabricated PIC).

integrated OF is implemented with a compact 4th-order distributed feedback resonator (DFBR) architecture, realized in a silicon strip waveguide Bragg grating (BG). The filter can be continuously tuned by controlling through local micro-heaters the optical path of four coupled cavities embedded within five BG mirrors [4], and thermally controlled Mach-Zehnder interferometers realizes the VOS/VOC structures. An air-filled deep etch trench (DET) through the full stack and down 60 μm into the silicon substrate is placed within the layout to improve the thermal isolation of the integrated OF and mitigate its wavelength drift as the RF/bias driving conditions of the PM-based OFC source are adjusted.

MATCHING NETWORK DESIGN AND PCB REALIZATION

Parallel to PIC fabrication, a PCB to be wedge-bonded to the PIC, carrying both the input LO reference for OFC generation and the control signals for the different on-chip actuators, has been developed. Coupling of the microwave signal with the DC reverse bias of the SiP modulator pn-junction is performed through an on-board bias tee. Since the comb source benefits from driving the SiP PM with large voltage values and considering power dissipation due to RF and DC bias signals at the termination load of the traveling-wave line realized above the modulator, a custom design for the bias tee able to support power levels of up to about 1.5 W has been adopted. The matching network is designed to operate in proximity of the SiP modulator cut-off frequency, which is about 20 GHz at the typical operating reverse-bias voltage levels of ~4 V. This allows attaining the mm-wave band with a relatively low multiplication factor of the input LO frequency, which helps in keeping the optical power of the selected OFC tone sufficiently large. A relatively broad range of about 8 GHz around this value has been also pursued for the operating frequencies, which can be advantageous for flexible selection of f_{LO} or in presence of wideband modulated RF driving signals [6]. The effect of wedge-bonds has been included in the model according to [7]. The results of the first guess design simulations of the interconnection including bias-tee are reported in Fig. 2(a), where the S_{11} and S_{21} parameters under variations around nominal values of the wedge-bond lengths as well as of the load impedance for the traveling-wave circuit carrying the modulator driving signal, are reported. A return loss below about 10 dB over a 18-26 GHz range is provided by simulations under the different load and wedge-bond length conditions. The PCB layout and a picture of the fabricated structure are also shown in Fig. 2(b). Contact pads are realized at the RF port for mounting a K-type connector to input the LO signal and the relevant transition between circuit microstrip and coplanar lines has been optimized too.



(a) (b)

Fig. 2. (a) Simulated S_{11} and S_{22} parameters of the on-board interconnection including bias tee under different (right) wire-bond lengths and (left) PM load impedance; (b) Layout of the designed PCB and micrograph of fabricated sample.

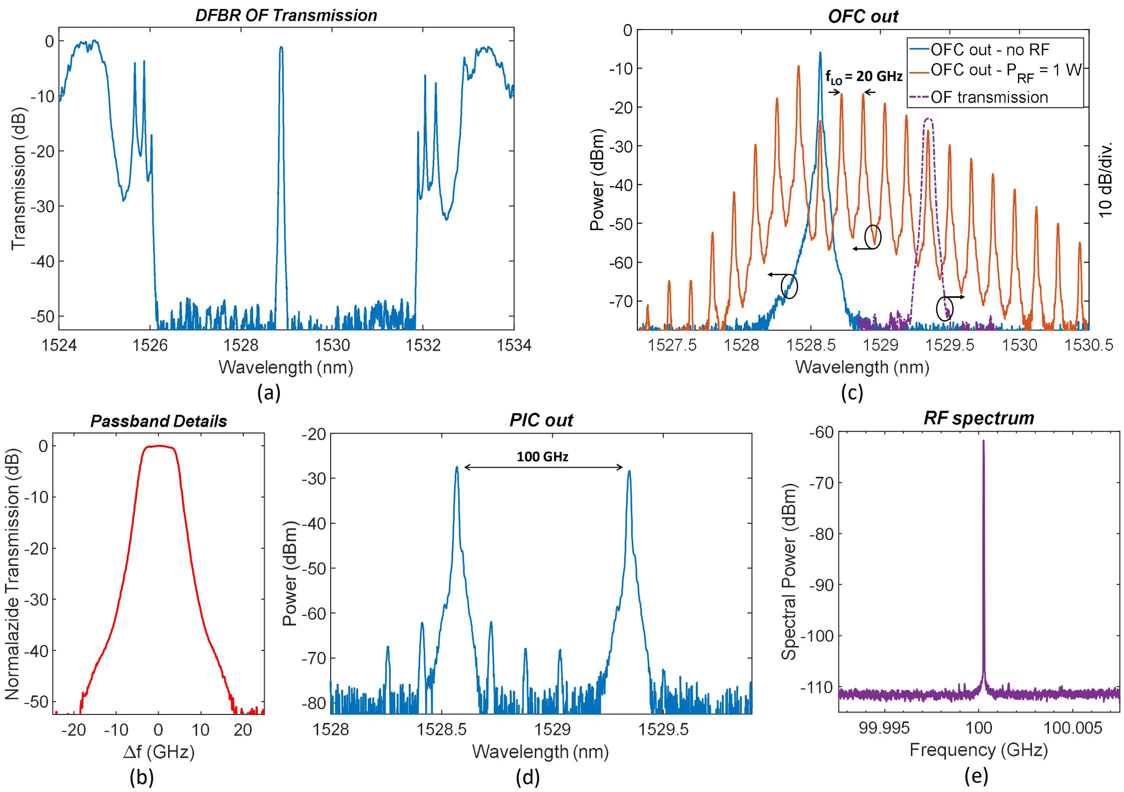


Fig. 3. (a) Full-span DFBR OF transmission; (b) Details of passband peak versus normalized frequency; (c) OFC source output spectra; (d) Optical spectrum at PIC output; (e) RF spectrum of generated 100 GHz clock.

PIC CHARACTERIZATION RESULTS

Preliminary on-chip testing of the circuit components and full-scheme operation is then performed. The measured transmission of the DFBR OF over a wide wavelength span, and the details of the transmission window in the center of the 6 nm-wide filter stopband are reported in Fig. 3(a) and (b), respectively. The passband peak exhibits a small insertion loss of ~1 dB, with a –3 dB width of about 8.5 GHz, and a rejection as large as 50 dB at 20 GHz from the central frequency. The spectrum at the output of the PM-based OFC generator is then shown in Fig. 3(b), when f_{LO} is 20 GHz and the driving power delivered to the RF probes contacting the modulator electrodes is ~ 30 dBm. The output carrier without applied RF signal is also shown, as well as the shape of the OF tuned in correspondence of the 5th-order longer-wavelength modulator sideband, spaced by 100 GHz from the input laser carrier. The optical spectrum of the composite signal (i.e., selected sideband and re-inserted carrier) at the PIC output is then shown in Fig. 3(d), illustrating a large minimum suppression of the spurious harmonics of about 34 dB. The corresponding RF spectrum of the synthetized 100 GHz continuous-wave signal, obtained through heterodyne detection with harmonic mixers in a signal spectrum analyzer is also reported in the figure.

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