EUROPEAN CONFERENCE ON INTEGRATED OPTICS

# Photonic memory based on $VO_2$/Si technology

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**In this work, we report a photonic memory in silicon photonics by exploiting the insulator-metal hysteresis of vanadium dioxide ($VO_2$). Our photonic memory based on a 5-µm-long $VO_2$/Si waveguide is maintained using ~150 µW of optical power, and can be on-chip written/erased using standard silicon building blocks.**
***Keywords***: *photonic memory, vanadium dioxide, silicon photonics*

## INTRODUCTION

Optical data storage in integrated optics has become an intense research topic in recent years, motivated by the possibility of achieving parallel operation with ultralow latency using light [1]. Such features are required to overcome one of the bottlenecks that limit classical von Neumann computation architectures using electronic circuitry, i.e., the interconnection between the processor and memory. However, light-based interconnections between the processor and memory require optical/electrical conversion. Hence, photonic memories are highly appealing to remove such a limitation. Additionally, the emergence of integrated photonic artificial intelligence relying on non-von Neumann architectures [2] directly benefits from photonic memories due to the possibility of performing in-memory computing, i.e., running calculations in the memory element [3].

Integrating chalcogenide-based phase-change materials (PCMs), such as GST, is currently the most established way to enable memory functionalities in silicon photonic devices [4]. These compounds exhibit an inherited non-volatile response when they are changed between the amorphous and crystalline states. However, the phase change requires a high-temperature increase (~600 °C) followed by fast cooling (> 10 °C/ns) in the amorphization process [5]. In this context, an alternative PCM compound such as vanadium dioxide ($VO_2$) can overcome those challenging temperature requirements by offering a phase transition temperature near room temperature (~68 °C) [6], [7]. Although $VO_2$ is a volatile PCM, the memory effect can be achieved by harnessing their hysteretic insulator-metal transition (IMT), as recently demonstrated in hybrid $VO_2$/Si waveguides by electronic biasing the IMT [8]. On the other hand, $VO_2$ provides a unitary contrast in the complex refractive index in the near-infrared similar to GST [10].

In this work, we propose a photonic memory based on an ultra-compact $VO_2$/Si waveguide. In comparison with previous work [8], our approach is all-photonic since the memory state is changed and maintained using light and standard integrated photonic building blocks, surpassing the need to include specific electronic circuitry in the $VO_2$ to keep the memory state.

## RESULTS

The concept and working principle of the proposed integrated photonic memory is depicted in Fig. 1(a). The memory is based on a 500 nm x 220 nm silicon (Si) waveguide with a 40-nm-thick $VO_2$ patch on top. The length of the hybrid waveguide is 5 µm and is covered with $SiO_2$. The memory is optimized for the transverse-magnetic (TM) polarization to maximize the light-matter interaction between the evanescent field and $VO_2$. Memory effect is achieved by leveraging the photoinduced hysteretic IMT of the $VO_2$ (see inset of Fig. 1(a)). Hence, the memory is written/erased by modulating a continuous-wave signal (optical bias) with a certain optical power that is adjusted within the hysteresis response of the $VO_2$. When a writing pulse is delivered to the hybrid waveguide, the $VO_2$ changes from the low-loss insulating state to the high-loss metallic state. Once the pulse is removed, the $VO_2$ remains metallic due to the optical bias (written memory state). To recover the insulating state (erase the memory), the optical signal must be reduced below the bias threshold using a low power-erasing pulse.

Fig. 1(b) shows the experimental transmission response of the hybrid $VO_2$/Si waveguide (see inset of Fig. 1(b)) as a function of the optical power using a continuous-wave signal at 1550 nm. The IMT of the $VO_2$ was photothermally triggered. The injected optical power was controlled with an off-chip erbium-doped optical amplifier. The insulator-metal transition starts around 450 µW, whereas the insulating state is recovered when the optical signal is removed.

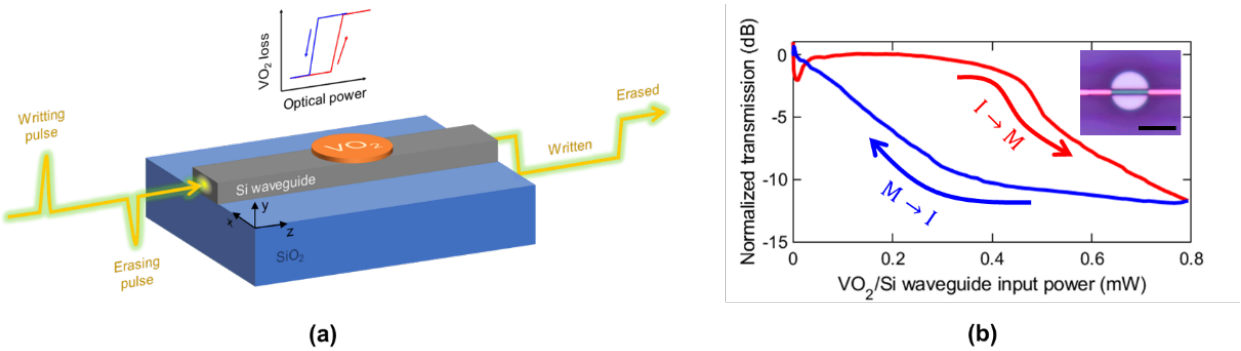


*Fig. 1. (a) Illustration and working principle of the proposed memory based on a hybrid $VO_2$/Si technology. (b) Transmission of the 5-µm-long $VO_2$/Si waveguide as a function of the optical power using a CW signal at 1550 nm. The hysteresis is obtained by sweeping back and forth the input power. The temperature of the chip was set at 20 °C. The inset shows a micrograph of the characterized hybrid waveguide. The scale bar is 5 µm.*

To demonstrate on-chip memory operation, we placed an asymmetric Mach-Zehnder interferometer (MZI) before the hybrid $VO_2$/Si waveguide. In this regard, writing (erasing) pulses could be achieved by changing the effective refractive index of the long (short) MZI arm. Fig. 2(a) shows an optical micrograph of the fabricated memory device comprising the MZI and the hybrid $VO_2$/Si waveguide before depositing the metallic heaters on top. The structures were patterned using e-beam lithography, and the $VO_2$ layer was deposited using molecular beam epitaxy. The chip was covered with a 1.4-µm-thick $SiO_2$ cladding. Then, 100-nm-thick titanium heaters and electrodes were fabricated by evaporation. The length of the microheaters was 80 µm.

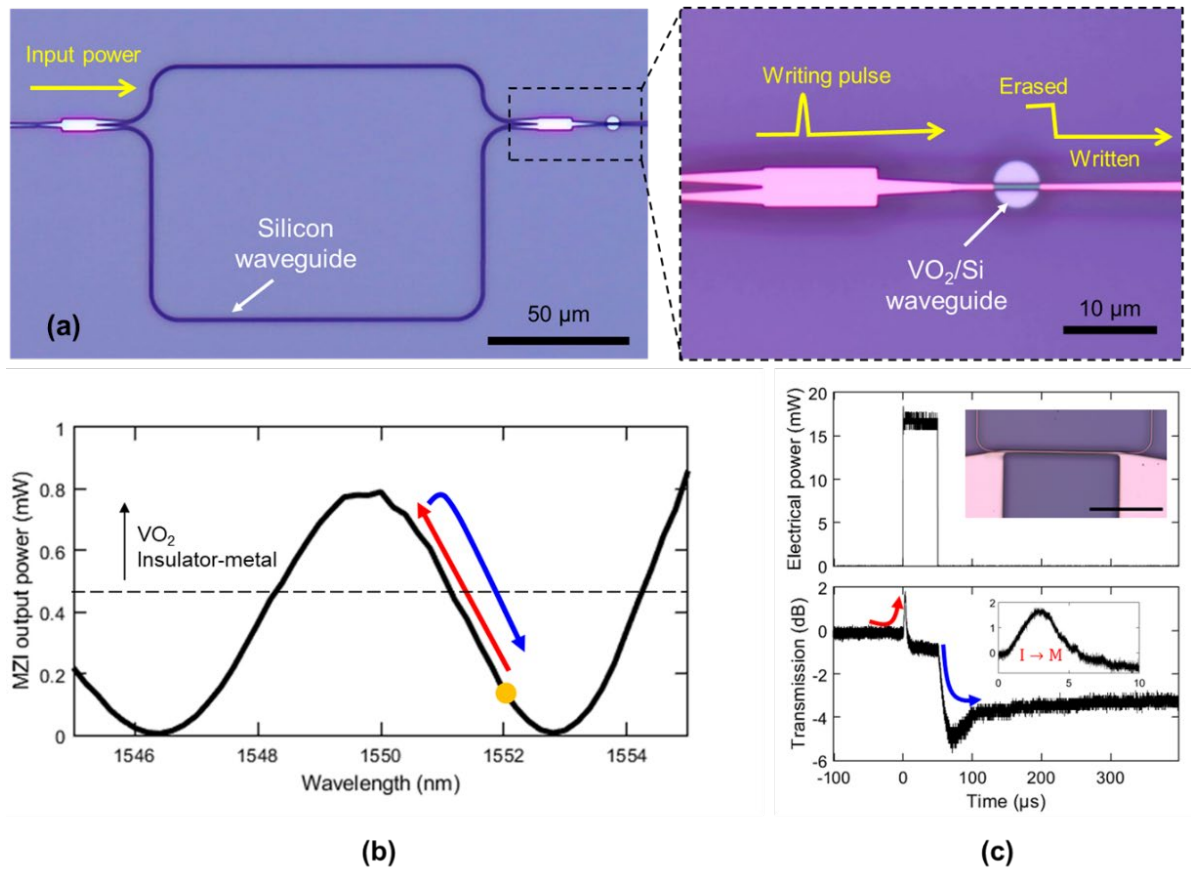


*Fig. 2. (a) Optical micrograph of the fabricated $VO_2$/Si memory using a MZI to on-chip write/erase the memory. A continuous wave signal with a certain bias, in both optical power and wavelength, is injected in the MZI to generate the writing pulse by heating the long arm and afterward keeping the memory written. (b) MZI spectral response when 1.6 mW optical signal is injected into the MZI. The dot stands for the operating wavelength utilized to write the memory. (d) Applied electrical pulse to the heater of the long arm (top inset, the scale bar is 50 µm) and normalized optical transmission of the memory when injecting 1.6 mW optical signal at 1552 nm.*

To demonstrate the memory function, the optical signal was set at 1552 nm (see Fig. 2(b)). For this value, the memory is in the erased state as we estimate around 150 µW of optical power delivered to the $VO_2$/Si waveguide in order to be within the hysteresis loop of the $VO_2$ (see Fig. 1(b)). The memory is written by applying an electrical pulse to the heater on the long arm of the MZI. In this manner, the optical response of the MZI is redshifted toward a maximum, and thereby the delivered power to the hybrid waveguide increases (inducing the insulator-metal transition) and changes the memory to the written state. The written memory state is maintained when the electrical pulse is removed due to the $VO_2$ hysteresis and the optical bias set by the selected wavelength and optical power of the input signal.

The temporal dynamics of a writing process are shown in Fig. 2(c) when a 50-µs-long pulse is applied to the heater of the MZI long arm (see Fig. 2(c) top inset). The electrical power of the pulse was ~17 mW (~4.5 V) in order to shift the MZI response toward one of its maximums. The normalized transmission of the memory can be seen in the lower graph of Fig. 2(d). Before applying the electrical pulse, the memory is erased with the $VO_2$ in the insulating state. Once the electrical pulse is applied, the transmission of the memory increases due to the redshift of the MZI until the $VO_2$ absorbs sufficient optical power to trigger its insulator-metal transition (see Fig. 2(c) bottom inset). Then, the optical transmission suffers a decrease caused by the optical losses induced by the metallic state of the $VO_2$. Upon the electrical pulse being removed, the transmission drops and is maintained (written state) because the MZI response returns to the original position (see Fig. 2(b)) while $VO_2$ remains in the metallic state.

**DISCUSSION**

In summary, we have proposed a photonic memory based on an ultra-compact hybrid $VO_2$/Si waveguide of just 5 µm length. The memory exploits the IMT hysteresis to provide a bistable response. Although the memory is volatile, the holding power required to maintain the memory written can be as low as 150 µW. On the other hand, the writing/erasing process could be achieved on-chip using standard silicon photonic building blocks such as thermo-optical controlled MZI. Such a memory device may be useful in photonic applications benefiting from in-memory computing neural networks or tensor cores.

Acknowledgments: Funding from the European Union's Horizon Europe by the granting Authority "HADEA (European Health and Digital Executive Agency) under Grant Agreement No 101070690 (PHOENIX). Grant PID2019-111460GB-I00 funded by MCIN/AEI/10.13039/501100011033, by "ERDF A way of making Europe". Grants 2-PAID-10-22 and 2-PAID-01-22 funded by Universitat Politècncia de València. Grant MS21-037 funded by European Union Next-Generation EU.

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