High-frequency Scalable Modelling of 100 GHz Class Uni-Travelling Carrier Photodiodes

Student paper

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In this paper, we demonstrate a scalable compact model to predict the performances of high speed UTC-PDs up to 110 GHz. Excellent agreement between the model and measurements has been achieved, allowing to find the optimal diode dimension for bandwidth up to 70 GHz.
Keywords: *UTC-PD, Predictive modelling, Optimization*

INTRODUCTION

With the continuous increase in data traffic, the need for high bandwidth optical receiver is growing. Uni-travelling carrier photodiodes (UTC-PD) are remarkable candidates as their operation relies only on electron transport [1]. We have recently reported high speed and high responsivity photodiodes of bandwidth above 70 GHz with 0.6 A/W responsivity [2]. In this paper, we focus on the development of a scalable model for these components capable to predict bandwidth up to above 70 GHz, which allows us to optimize PD geometry and determine the main limitation of photodiode structure for further optimization.

SCALABLE MODEL DEVELOPMENT AND RESULTS

S-parameter (S11) measurements up to 110 GHz under three bias points (-0.5V, -1V, -2V) were performed on our photodiodes of various dimensions and on their corresponding test structures following SOLT calibration. The parasitic effects of pads and transmission lines were removed using a de-embedding method described by Eq. (1) [3], where the inputs are the measured S-parameters of the diode (S_{meas}) and the related open (S_{OC}) and short circuit (S_{SC}) test structures.

$$S_{de-emb} = \frac{S_{OC} + S_{SC} - 2S_{meas} - S_{meas}(S_{OC} - S_{SC})}{2S_{OC}S_{SC} + S_{SC} - S_{OC} - S_{meas}(S_{OC} + S_{SC})} \quad (1)$$

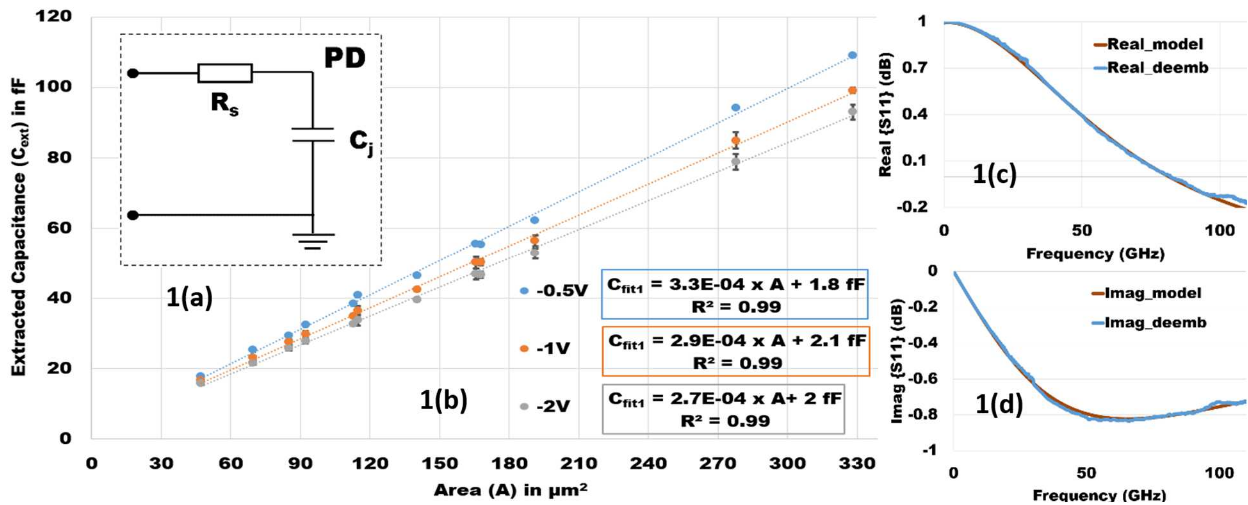

Figure 1(a) Equivalent circuit of the photodiode, 1(b) Extracted Capacitance vs Area of diodes at different bias, 1(c) Real and 1(d) Imaginary parts of S11 showing equivalent model fit with the De-embedded measurements for a 5x25µm² diode

Next we extract the parameters of the equivalent circuit (Fig. 1(a)) for each diode geometry in comparison with the de-embedded S-parameters. We plot the extracted values of the junction capacitance (C_{ext}) over surface from the model fitting (Fig. 1(b)), with standard deviation reported for the -1V and -2V curves, depicting linear area-dependence of the capacitance. A very good agreement between de-embedded measurements and the model is observed, as shown in In Fig. 1(c) and (d), for a 5x25µm^2 PD. The error bars in Fig.1(b) show the standard deviation

ranging between 0.3-2.1 fF. From the linear regressions, we can formulate Eq. (2) (reported for -2V), to model the scaling behavior of the junction capacitance (C_{fit1}).

$$C_{fit1}(-2V) = (2.74 \times 10^{-4} \times A) + (2 \times 10^{-15}) \tag{2}$$

From Eq. (2), we observe that there is a 2 fF parasitic capacitance independent of the surface area which roughly remains constant for all biases. To elaborate a geometry-dependence of the capacitance, we refer to the parameter scaling methodology associated with HICUM model [4] and write the extracted capacitance as shown in Eq. (3) in terms of the area (A) and perimeter (P), which is then transformed into Eq. (4)

$$C_{ext} = C_A . A + C_P . P \tag{3}$$

$$\frac{C_{ext}}{A} = C_A + C_P . \frac{P}{A} \tag{4}$$

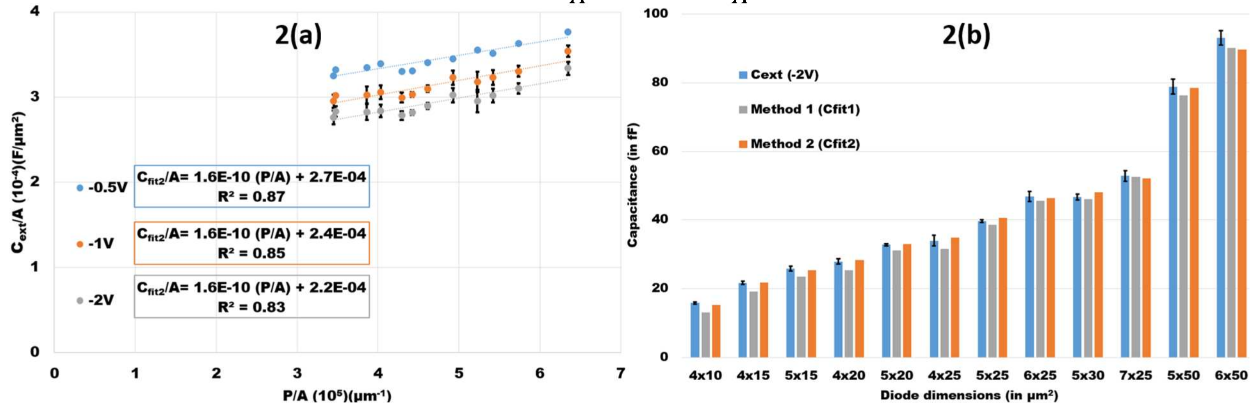

Figure 2(a) Dimensional capacitance contribution extraction plot, 2(b) Extracted and simulated capacitances at -2V

The normalized capacitance in Eq. (4) is plotted in Fig. 2 (a) as a function of the quantity P/A from which intrinsic capacitance C_A and perimeter-dependent component C_P can be extracted from the intercept and the slope, respectively, for different bias voltages as shown in inserts of Fig. 2 (a). We can observe that the perimetric contribution C_P is practically independent of the bias, hence it's not depend on PD junction, but on the surrounding (passivation, …). C_P plays a smaller contribution in bigger PDs and a larger part of capacitance in smaller PDs, with maximum of 20.5% for 4x10μm^2 PD. Fig. 2 (b) shows that method 2 gives better accuracy than method 1 for the capacitance, with error less than 1 fF. We can then estimate the depletion thickness, *d*, for each bias voltage from the C_A using the standard capacitance formula (eq. (5)) as listed in Table 1(a) that would be used, in turn, to calculate the transit times.

$$d_{@2V} = \frac{\varepsilon_0 \times \varepsilon_r}{C_{A@2V}} \tag{5}$$

d at each bias	Thickness in nm
-0.5V	437
-1V	504
-2V	549

Bias	f_{RC}_4x10	f_{RC}_4x15	f_{tr}	V_s_4x15
-1V	124 GHz	99.7 GHz	100 GHz	1.2×10^5
-2V	135 GHz	108 GHz	80 GHz	1×10^5

Table 1(a) Depletion layer thickness at each bias, 1(b) RC & transit cut-off frequency, electron velocity of diodes at different bias

In our photodiodes, we have a 440 nm collector (including undoped absorber and transition layer) followed by a 180 nm absorber gradually doped to boost photodiode transit time [1]. The strong bias dependence of the depletion width can be explained by the low doping of the absorber-collector interface.

The same scaling methodology is followed for the diode series resistance (R_{ext}). To have a linear model we convert extracted resistance into conductance (G_{ext}) for the analysis. In a similar manner as before, Eq. (6) can be obtained from the conductance vs P/A plot (Fig. 3(a)), where the slope and intercept give the perimeter-dependent component (G_P) and the intrinsic conductance (G_A), respectively. Using the scaling equation, we can recalculate the resistance, as shown in Fig. 3(b) along with the extracted resistance, depicting very good agreement.

$$G_{fit}(-2V) = (3.4 \times 10^8 \times A) + (8 \times 10^2 \times P) \tag{6}$$

Once the scaling rules for the diode R-C elements are accurately extracted, we can model the full frequency response (Fig. 4(a)), by calculating the transit time using the standard UTC-PD photocurrent equation [1] together with the equivalent circuit shown in Fig. 4(b). With the known the values, we readjusted the electron velocity in the collector (V_{s1}=1.2x10^5 and V_{s2}=1x10^5 for -1V and -2V, respectively) to obtain a better fit the measured bandwidth.

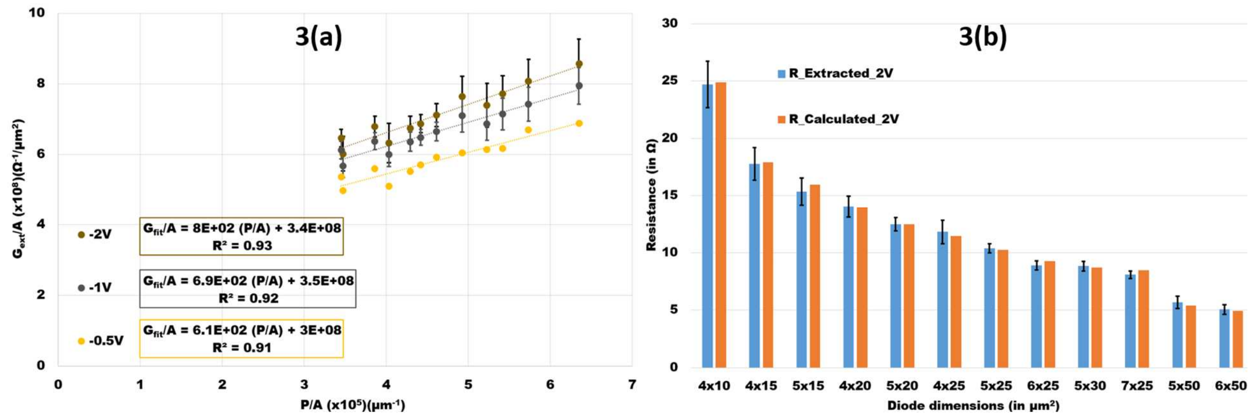

Figure 3(a) Dimensional conductance contribution extraction plot, 3(b) Extracted and simulated resistances at -2V

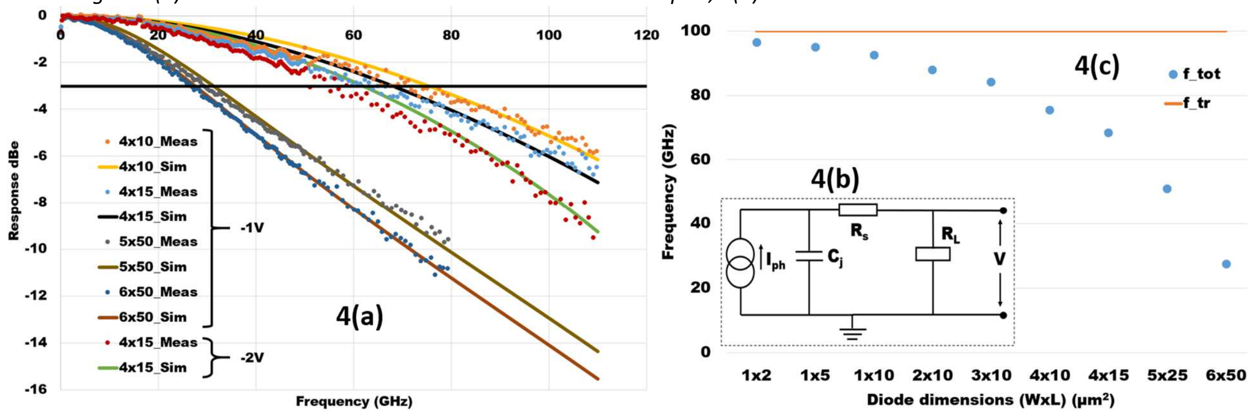

Figure 4(a) Frequency response of PDs of different dimension (in µm²) at different bias 4(b) Equivalent circuit for RC response 4(c) Response of extrapolated dimensions using our predictive model

With the same electron velocity at -1V, we simulate responses of various diodes under 1mA photocurrent (I_{ph}) in Fig. 4(a), showing good agreement between simulated data and the measured response. We also compare measured and simulated frequency responses of a 4x15µm^2 photodiode at -1V and -2V. From the measured response, we see that the 3dB bandwidth is around 62 GHz at -1V, and around 57 GHz at -2V for 4×15 µm² PD and 71 GHz at -1V for 4×10 µm² PD. Transit times of the diodes are listed in Tab. 1(b). Note that the variation of electron velocity is the dominant factor for transit time limited response; hence higher bandwidth can be obtained by reducing the collector thickness. From our model, Fig. 4(c) shows that maximum bandwidth is 100 GHz and that below 2x10µm^2 (88 GHz) bandwidth improvement is negligible. To improve further, reducing the collector thickness is the only way.

CONCLUSION

We have demonstrated a scalable modeling approach for the R-C parameters in UTC-PDs, which can accurately capture the high-frequency behavior of the device and can be used for predicting its physical characteristics through geometrical extrapolation of parameter values. The model has been validated for a wide range of dimensions and bias voltages. The benefit of our proposed scalable model lies in its use in future designs especially to accurately and reliably predict the high-frequency performance of scaled devices. From our predictive model, we have shown that our structure can reach up to 88 GHz bandwidth. In future iterations of this work, we plan on further exploring the scalable model for predictive simulation in the context of optoelectronic integrated circuits.

References

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