Fully Integrated Quasi-Coherent Receiver Based on Co-hosted InP PIC and a SiGe ASIC

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A co-hosted quasi-coherent receiver involving a monolithic indium phosphide PIC and a fully integrated 30 GHz TIA and envelope detector ASIC is demonstrated and characterized for both C and L bands. Optical filterless channel selection is studied.
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INTRODUCTION

The ever-growing demand for bandwidth due to higher data center traffic requires improved networks that can grow organically with the needs. In today's network structure, the connection to the end user is typically in a point to multi-point manner through Passive Optical Networks (PON). PONs have evolved rapidly over the past few decades reaching mass deployment of 10 Gbit/s technologies and providing the first demonstration of 50 Gbit/s electro-optical implementation [1], [2]. This evolution has been achieved through the efforts of standardization bodies, maintaining basic principles such as coexistence, the use of intensity modulation (IM) or the maintenance of a high link budget, and in some cases the introduction of wavelength division multiplexing (WDM).

While network capabilities are improving, deployment costs are not expected to increase linearly with complexity, leading to a search for more powerful, albeit simpler, electro-optical hardware solutions. A winning path for such a search is the use of Photonic Integrated Circuits (PICs). Efforts to develop generic photonic integration processes have been developed globally, fostering the PIC ecosystem and increasing the maturity of the technology, and reducing the entry cost [3].

The use of a coherent receiver, i.e., a receiver architecture that is capable of recovering not only amplitude information but also its phase through the use of a local oscillator (LO) has been presented to achieve enhanced performance in future networks [4]. Coherent reception brings additional sensitivity i.e., extra power budget and higher bit rate while simultaneously using phase and amplitude schemes and channel tunability. These advantages arise from using the local oscillator which represents an attractive feature for WDM systems. Plenty of work has been carried out and reported to develop Application Specific Integrated Circuits (ASICs), co-packaged together with discrete optics when using IM alongside coherent detection. In this scenario, the receiver can reach demodulation bitrates up to 28 Gbit/s [5]. Along the same path of innovation, receivers for networks using IM based on PIC have also been proposed and reviewed [6], [7].

This paper presents the ultimate step towards the successful development of transceivers with quasi-coherent receivers that can be used in cost-sensitive networks, i.e., the fusion of a dedicated PIC and an ASIC in the same package. A quasi-coherent receiver leverages coherent detection, above mentioned, to detect only the amplitude while discarding the phase information of the received signal. The developed solution includes an electro-optical receiver based on a fully monolithic Indium Phosphide (InP) PIC co-hosted with a Silicon Germanium (SiGe) ASIC. It is designed to implement coherent detection for IM, which allows the receiver to act as a WDM filter while featuring polarization independence. The ASIC and PIC are co-packaged using a multi-pocket host of Silicon (Si) and the monolithic PIC was designed and fabricated to support both the C and L bands.

Co-hosted device and experimental setup

Fig 1 a) shows a detailed image of the co-hosted InP PIC + SiGe ASIC, through a proprietary Si multi-pocket which is thermally and mechanically connected to a custom Printed Circuit Board (PCB). The bottom layer of the device is a Thermoelectric Cooler (TEC) that is externally controlled to maintain the co-hosted device at the targeted temperature. The Si host contains slots for the ASIC and PIC and is geometrically designed to match the PIC and ASIC input/output interfaces and dimensions while minimizing the distance between their high-speed interfaces. The host also includes electrical traces and pads for the various interconnections required between the integrated
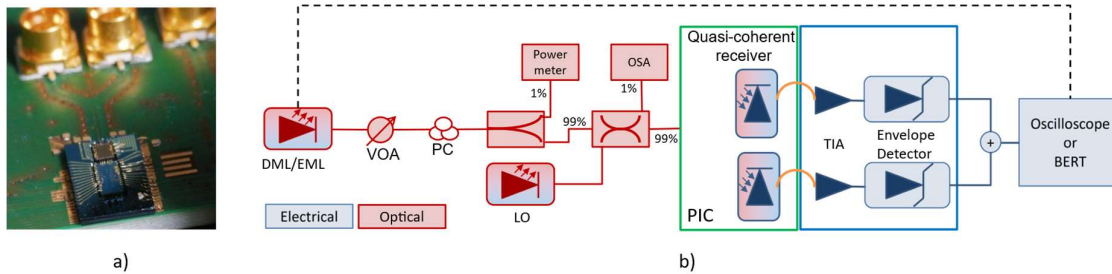
Fig. 1. a) Detailed image of the co-hosted InP PIC and SiGe ASIC. b) Block diagram of the device under test (DUT) and setup.

circuits and the PCB as well as V-grooves for fiber alignment. Wire bonds between the PIC and the ASIC connect the high-speed output of the PIN photodetectors to the input stage of the ASIC's transimpedance amplifier (TIA). The output of the ASIC is wire-bonded to the Si host RF lines designed and fabricated to provide a bandwidth of more than 30 GHz with an insertion loss of less than 1 dB. The host RF lines are then wire- bonded to the PCB RF lines.

The remaining DC electrical connections are made from the PIC /ASIC to the Si host through wire-bonding. The InP PIC was designed using the Fraunhofer Heinrich Hertz Institute (HHI) generic integration processes [8]. It features a simplified quasi-coherent architecture, capable of detecting the signal amplitude [9]. A LO used in heterodyne regime is mixed with the input signal and then split into two PIN receivers with equal amplitude and orthogonal components to achieve polarization independence. The electrical output signals from the coherent receiver feed the ASIC whose input stage is a high-speed linear TIA, followed by an envelope detector to downconvert the signals to baseband. The final stage comprises the electrical combination of the two components.

Fig. 1 b) shows the setup used to characterize the device. The green box represents the PIC which contains an LO and the quasi-coherent receiver with two PIN photodiodes and the blue box contains the ASIC, comprising the two TIAs and the necessary envelope detectors. The architecture also allows the use of an external LO. The input signal to the receiver is generated through a commercially available XFP and its evaluation board [9],[10], which is fed by a modulated signal generated with the Bit Error Rate Tester (BERT) ExoBERT2904 with 2^7 -1 Pseudo Random Sequences (PRBS) at 10 Gbit/s. The output signal from the transmitter goes through a polarization controller (PC) that locks the state of polarization through the measurements and feeds a 99%/1% 2x2 coupler used as a monitor. The remaining input of the 2x2 coupler is fed with an external tunable laser APEX AP3350A/3352A with wavelengths from 1526-1608 nm and ~300 kHz linewidth, this laser is used as external LO covering the bands under study on this paper. The optical interfacing is performed through a cleaved Standard Single Mode Fiber (SSMF) and a Spot Size Converter (SSC) at the PIC side. The differential electrical ASIC's output of the recovered signal is then connected to the Exo-BERT 2904 for real-time Bit Error Rate (BER) measurement or a digital scope TEKTRONIX DSA72004.

Experimental Results

The results shown in fig. 2, present the characterization of the implemented receiver in the context of WDM operation. The device working bandwidth was measured through the detection of a 10 Gbit/s signal, generated by commercial grade ONU (λ = 1532 nm DML) and OLT (λ = 1595 nm EML) NGPON-2 transceivers [10]. The eye diagrams from Fig.2 a) are shown for the optimal point of 10 Gbit/s operation. Starting from the ideal heterodyne frequency, ~22 GHz, the LO was swept so that we could access the optical power penalty for the BER of 10E-3, Fig 2b).

The measured device working bandwidth, indicated by the green arrows in Fig.2 b), is 9 GHz for C band (DML) and 13 GHz for L band (EML), showing the tolerance of the system to a lower cost commercial transceiver (DML), with the difference between each case being justified by the broader spectrum of the DML. Both cases are limited by the bandwidth of the ASIC (30 GHz). After testing the receiver's performance using one single wavelength channel, additional DML transmitters operating at other NGPON2 channels spaced according to the ITU-T grid were added to the setup shown in Fig. 1 to evaluate the performance and filter capabilities of the receiver when receiving multiple wavelength channels simultaneously. Fig. 2 c) compares, for a given measured BER value when transmitting CH1 (1532.68 nm, -10 dBm at the PIC input), the power penalty required to obtain the same BER value when simultaneously transmitting the desired IM signal through CH1 and another 10 Gbit/s IM signal in the adjacent channel CH2 (1533.47 nm) with different optical output powers of -5, 0 and +5 dBm. The observed power penalty is 1 dB when CH2 is emitting at -5 or 0 dBm and 1.5 dB when CH2 emits +5 dBm of optical power.
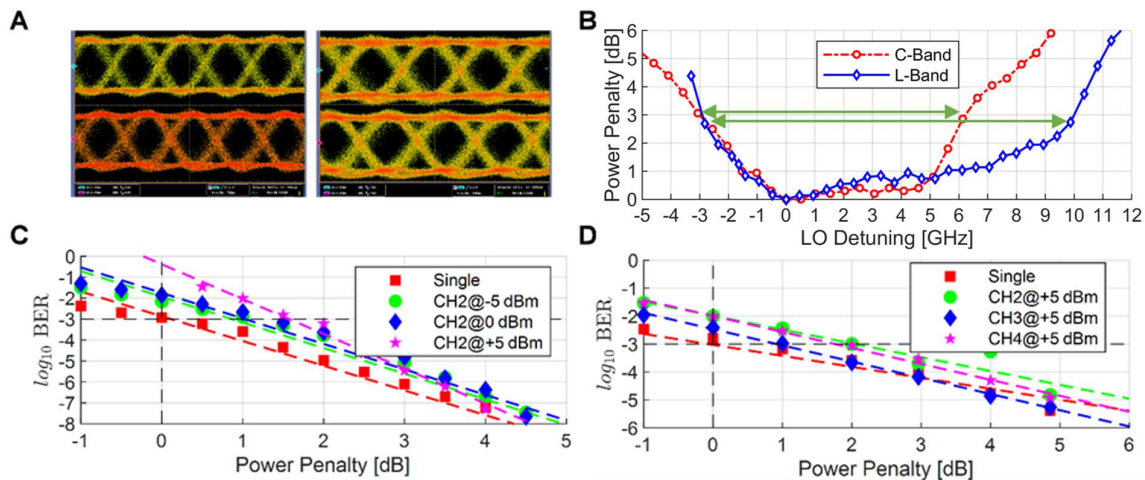
Fig. 2. a) Recovered eye diagrams for 10Gbps, b) Power penalty as a function of the LO frequency detuning for 10Gbps, c) Power penalty associated with different output powers, d) Power penalty associated with different propagating channels through 10km of SSMF

The same study was performed by including a 10 km optical fiber spool and adding other transmitters, CH3 (1534.25 nm) and CH4 (1535.04 nm). The results, depicted in Fig. 2 d) show that when CH2 or CH4 emit at the highest power (+5 dBm), there is 1 dB of power penalty between the CH1 (stated as Single) and CH4 and 2 dB between CH1 and CH2 which is the most adjacent channel, proving the filter and tuning capabilities of the quasi-coherent receiver presented in this paper.

Conclusion

A co-hosted InP Photonic Integrated Circuit, PIC, and SiGe ASIC receiver for quasi-coherent reception of IM modulated signals was demonstrated. The implemented system demonstrates its ability to demodulate 10 Gbit/s IM modulated signal at the specified NGPON2 channels. Using commercially available transmitters in the C (DML) and L (EML) bands, the device working bandwidth was measured by LO detuning. This test allowed to demonstrate the device capabilities of working with different types of transmitters and its wideband operation. It also demonstrated the filtering capabilities of the prototype when adjacent channels are simultaneously used, targeting WDM systems.

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