Design of III-V on Silicon Optical Switch based on Mach-Zehnder and SOA Switching Elements

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Abstract

This work proposes a novel lossless photonic switch based on III-V semiconductor optical amplifiers (SOAs) combined with Si-photonics in a heterogenerous integration scheme. An 8×8 device implemented using dilated Banyan topology achieves a 17dB input power dynamic range (IPDR) with power penalties of less than 1dB. A 64×64 Clos switch built from the 8×8 blocks exhibits a 10dB IPDR with power penalties of less than 1dB.

Introduction

Optical Space switches based on 3D-MEMS requires rigorous calibration and introduces significant complexity. [2] To ensure low cost for eventual data-center adoption, Many integrated technologies are favored. [1] Indium phosphide (InP) and silicon based integration technologies have been widely explored with significant advancement in the last decade. However, further scale-up is bounded because of large footprint InP devices [6], and silicon photonics is limited by the intrinsic passive loss.[1] In this work, we propose the heterogenous integration to design an 8×8 III-V on silicon switching building block.

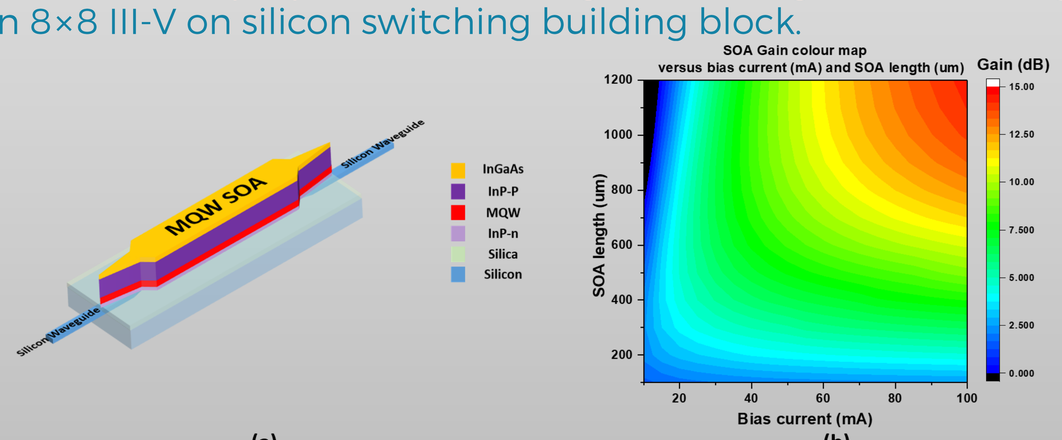

Figure 1. (a) The configuration of the heterogeneous integration of III-V on silicon SOA with double adiabatic coupling taper ; (b) SOA gain color-map versus SOA length and bias current at -5dBm switch on-chip input power.

8×8 Gain-integrated silicon building block

An adiabatic coupling taper [5] is used in the design to minimize the coupling loss from the underlying silicon waveguide to the upper layer where III-V SOAs are bonded. The signal is amplified then coupled back into the silicon waveguide via a second taper.

A fundamental switch building block is formed by dilated Banyan architecture as a strictly non-blocking switch fabric. [4] The binary dilated arrangement in the architecture provides a good isolation for below -60dB crosstalk. SOAs on silicon using heterogeneous integration in the middle stage can compensate the insertion loss for every path and further suppress the crosstalk with an additional -30dB extinction ratio. An 900μm long SOA with 40mA bias current has 11.0dB gain to compensate for the total loss of an optical path.

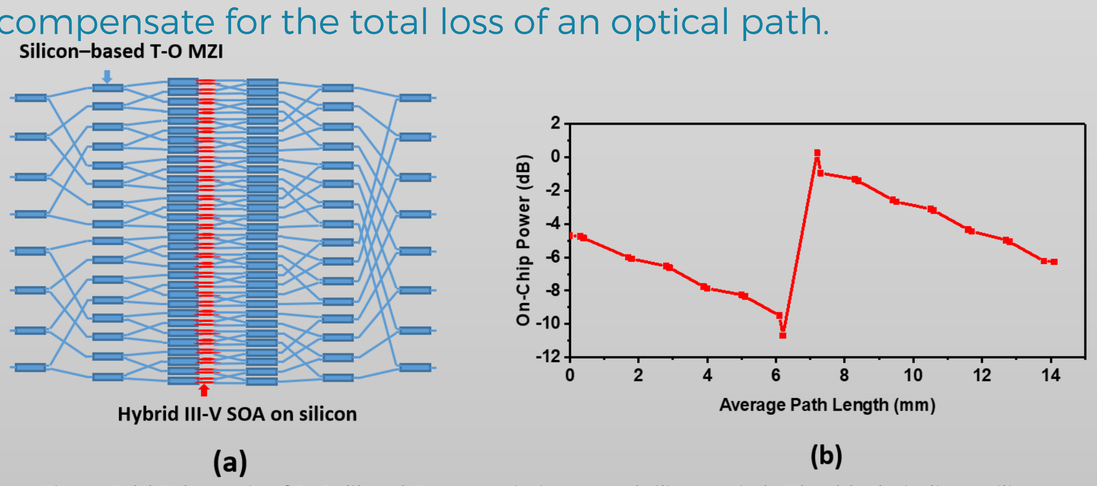

Figure 2. (a) Schematic of 8×8 dilated Banyan gain-integrated silicon switch. Blue blocks indicate silicon-based T-O MZ silicon switches and the red shapes represent heterogeneous integration (b) On-chip power estimation for path in average for 8×8 dilated Banyan switch.

The component-level loss is initially estimated to determine the on-chip gain required for the SOAs. The input power is set as -4.7dBm resulting in an output power -6.3dBm.

8×8 building block and 64×64 Clos switch performance

By using the proposed 8×8 switch building block, a 64×64 Clos switch fabric can be achieved to make a large port count fast switch. The simulation work shows there is a low power penalty and wide IPDR at power penalty less than 1dB when a 10Gb/s non-return to zero (NRZ) modulated optical signal at 1550nm transmitted as an input of the device.

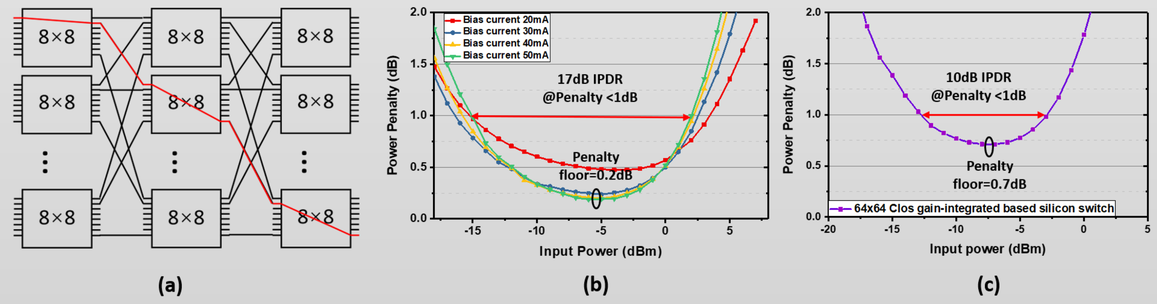

Figure 3. (a) Schematic of 64x64 Clos Switch built by 8x8 designed building blocks, the red line represents an arbitrary switch path via three Clos stages ; (b) Power penalty at BER of 10-9 versus switch on-chip input power for 8x8 gain-integrated silicon switch; c) Power penalty at BER 10-9 versus switch on-chip input power for 8x8 dilated Banyan silicon switch;

- The worst-case loss and crosstalk are considered in the model
- 8x8 dilated Banyan switch building block performance assessment
  - ✓ Power penalty floor is 0.2dB at a BER of 10^{-9}
  - ✓ 17dB IPDR with a penalty less than 1dB is achieved.
- 64x64 Clos switch performance assessment
  - ✓ Power penalty floor is 0.7dB at a BER of 10^{-9}
  - ✓ 10dB IPDR with a penalty less than 1dB is achieved.

The design can be applied to larger switch network due to its relatively low power penalty.

Conclusion

This work describes a new gain-integrated 8×8 silicon MZ switch design. Evanescently coupled SOAs elements and silicon-based T-O MZ switch units are used and assembled in dilated Banyan topology providing a strong suppression.

This work for the first time proposes and assesses the design of a 8×8 gain-integrated silicon switch building block, showing a 0.2dB power penalty floor at 10^{-9} BER and a 17dB IPDR for 1dB penalty. A 64×64 Clos switch is subsequently modelled exhibiting a 0.7dB penalty floor and 10dB IPDR with power penalty less than 1dB. Further work is currently doing with a chip fabrication process.

References

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