Design of III-V on Silicon Optical Switch based on Mach-Zehnder and SOA Switching Elements

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ABSTRACT

This paper proposes a novel lossless photonic switch based on III-V semiconductor optical amplifiers (SOAs) combined with silicon photonics in a heterogenerous integration scheme. An 8×8 device implemented using dilated Banyan topology achieves a 17dB input power dynamic range (IPDR) with power penalties of less than 1dB. Silicon-based thermo-optic (T-O) Mach-Zehnder (MZ) switching elements are used to manipulate light, whilst SOAs are placed in the middle to switch in tandem with the MZs to provide gain and crosstalk suppression. A 64×64 Clos switch built from the 8×8 blocks exhibits a 10dB IPDR with power penalties of less than 1dB.

Keywords: Integrated optical devices; silicon photonics; optical switching

1. INTRODUCTION

The exponential growth of network traffic in data centres places high scalable, low power consumption and low latency demands on optical interconnects. Photonic switches can act as an alternative to support growing bandwidth requirements as a result of the increasing scaling trend and high bandwidth density at both switch and link level [1]. To realise dynamic and reconfigurable networks, compatible, robust, fast and flexible optical switches are therefore required.

Optical space switches based on micro-electromechanical systems (MEMS) represent the most mature and commercial technologies; however, their rigorous calibration introduces significant complexity that is ultimately reflected in the cost per port [2]. To ensure low cost for eventual data-center adoption, integrated technologies are favoured [1]. Indium phosphide (InP) and silicon based integration technologies have been widely explored with significant advancement being achieved in the last decade. A few thousands of components have been monolithically integrated on the InP platform for a lossless SOA-based 16×16 port count switch [3] and a space-and-wavelength switch with 64×64 connectivity [4]. However, further scale-up may be bounded by the relatively large footprint of InP devices [5]. On the other hand, silicon photonics attracts attention as it offers the benefits of small footprint, energy efficiency, and CMOS manufacturing compatibility. While this type of technology has been demonstrated with very large-scale integrations with over a hundred port counts for optical switching circuits [5], the ultimate limitation is revealed as the intrinsic passive loss [1]. Currently, new research opportunities have been identified to accomplish gain integration into the silicon platform, via hybrid or heterogenous integration schemes. Whereas initial demonstrations of gain-integrated silicon switches tend to apply a hybrid integration approach where III-V dies are flip-chip bounded on top of a silicon carrier [6], this method requires a very precise alignment process and also has reflection issues at interfaces. In addition, it lacks flexibility in the switch design as the etched silicon cavity can be either placed at the front-end or back-end of the device. Heterogenous integration via wafer or die bonding techniques, however, provides a more powerful way for implementing gain in Si Photonic optical switches.

In this paper, we design an 8×8 III-V on silicon switching building block using a dilated Banyan topology and perform physical-layer simulations. An adiabatic coupler is deployed to couple the light from the underlying silicon waveguide to the SOA, which provides an optical gain to compensate the passive losses in silicon. A Clos topology is then applied to achieve a 64×64 switch fabric. Simulation results indicate that this new 8×8 gain-integrated silicon switch exhibits a very wide (IPDR) with power penalty less than 1dB and the 64×64 Clos silicon switch still achieves a reasonably wide IPDR of 1dB penalty.

2. 8×8 GAIN-INTEGRATED SILICON BUILDING BLOCK FOR A 64×64 CLOS SWITCH FABRIC

Figure 1(a) shows a schematic of heterogeneous integration of a III-V multiple quantum well (MQW) SOA on silicon. Optical signals couple from the underlying silicon waveguide to the upper layer where III-V SOAs are bonded via an adiabatic coupling taper [7]. At the end of the SOA section, the amplified signals couple back into the silicon waveguide via a second taper.

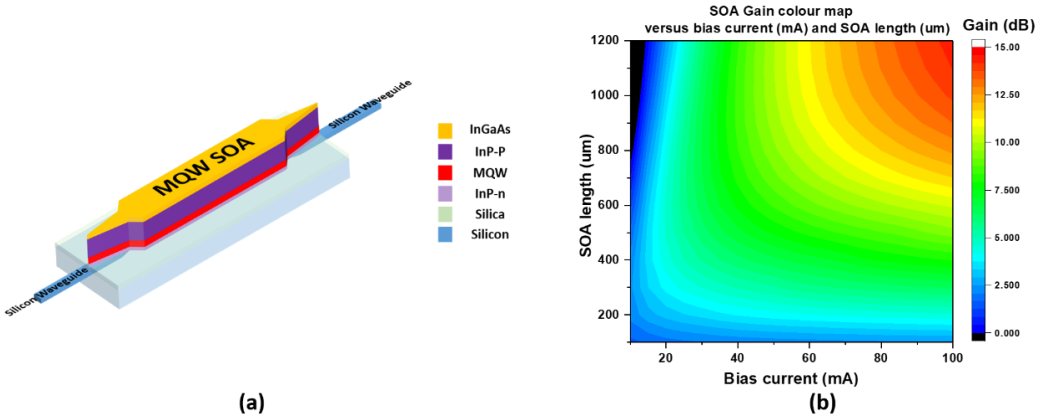

Figure 1. (a) The configuration of the heterogeneous integration of III-V on silicon SOA with double adiabatic coupling taper ; (b) SOA gain colour-map versus SOA length and bias current at -5dBm switch on-chip input power.

This heterogeneous integration introduces optical gain by the integrated SOA elements. However, the confinement factors of MQW and separated confinement heterostructure (SCH) are 0.035 and 0.15, respectively [8], which are lower relative to a typical stand-alone III-V based SOA (0.06 and 0.56) [12]. The optical gain as a function of SOA length and bias current is thus investigated using the VPI simulator [12] to determine the optimal design of the SOA block in the 8×8 integrated switch. The colour map in Figure 1(b) shows optical gain at device lengths from 100μm to 1200μm and bias currents from 10mA to 100mA at -5dBm input optical power. A 900μm long SOA is selected as it has a sufficient gain to compensate for the total loss of an optical path while with limited excess noise. In this simulation, we consider a worst-case scenario for silicon-based thermo-optic MZ switches, where the target length of the MZ phase shifter is 1mm and silicon waveguide loss is 1.5dB/cm [9]. An MZ switching elements has loss of less than 1dB and crosstalk of -20dB in our simulation although current engineered MZ switch has lower 1dB loss and crosstalk as low as -28dB [9]. In addition, Silicon waveguide crossing induces a 0.05dB loss and crosstalk of -40dB [10].

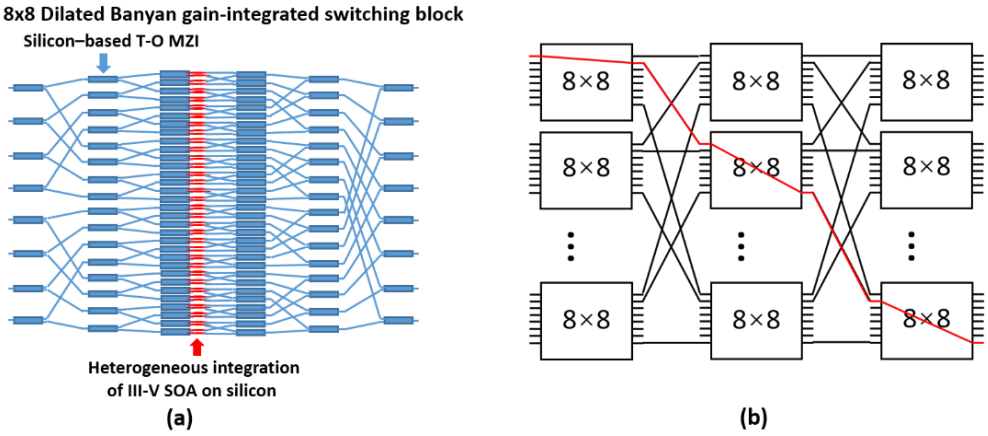

Figure 2. (a) Schematic of 8x8 dilated Banyan gain-integrated silicon switch, Blue blocks indicate silicon-based T-O MZ silicon switches and the red shapes represent heterogeneous integration of SOAs on silicon (b) Schematic of 64x64 Clos Switch built by 8x8 designed building blocks, the red line represents an arbitrary switch path via three Clos stages.

An 8×8 dilated topology is therefore chosen to suppress the crosstalk from the MZ switch units. Dilated Banyan architecture as a strictly non-blocking switch fabric [11] is implemented in this design which provides simple physical arrangement, logical equivalence and decreased waveguide crossings. Figure 2(a) describes the switching element in this design, where the binary dilated arrangement in this architecture provides a good isolation between adjacent paths for below -60dB crosstalk. In addition, an array of SOA elements bonded in the middle stage can compensate the insertion loss for every path and further suppress the crosstalk with an additional -30dB extinction ratio by providing strong absorption in the OFF state. Therefore, by using the proposed 8×8 switch building block, a 64×64 Clos switch fabric can be achieved.

3. 8×8 GAIN INTEGRATED BUILDING BLOCK AND 64×64 CLOS SILICON SWITCH PERFORMANCE

To assess the performance of the 8×8 switching building block and 64×64 Clos silicon switch, the component-level loss is initially estimated to determine the on-chip gain required for the SOAs . The 900μm-long SOA biased

with 40mA provides 11.0 dB optical gain, as shown in Figure 3(a), where on-chip power decreases because of passive silicon waveguide, waveguide bends and crossings, and MZ switch losses. The input power is set as -4.7dBm resulting in an output power -6.3dBm. In this work, the performance of silicon switch is simulated with parameters fitted from references and the design shuffle network crossing and bend numbers. A 10Gb/s non-return to zero (NRZ) modulated optical signal at 1550nm is transmitted as an input of the device. The worst-case loss and crosstalk are considered in the model, and the influence of 4 different bias levels is investigated. Figure 3(b) depicts the power penalty at a bit error rate (BER) of 10^{-9} versus input optical power. A 0.2dB power penalty floor and 17dB IPDR with a penalty less than 1dB are achieved when bias current is set to 50mA.

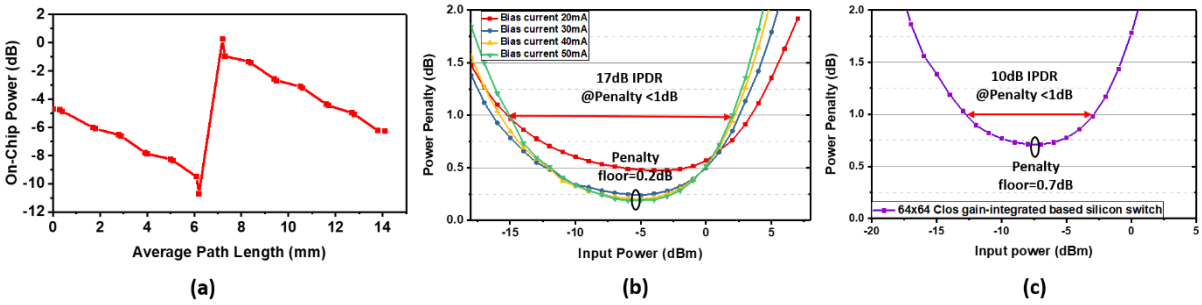

Figure 3. (a) On-chip power as a function of switch path length in average for 8x8 dilated Banyan heterogeneous integrated silicon switch; (b) Power penalty at BER of 10^{-9} versus switch on-chip input power for 8x8 gain-integrated silicon switch; c) Power penalty at BER 10^{-9} versus switch on-chip input power for 8x8 dilated Banyan silicon switch;

The component-level 2.2dB average loss induced by waveguide crossings and bending from 64×64 Clos shuffle networks are considered in this model. Simulation results for the 64×64 switch, where three Clos cascading stages include identical 900μm SOAs biased at 50mA, are shown in Figure 3(c). An IPDR of 10dB with power penalty less than 1dB is achieved.

4. CONCLUSION

This paper describes our recent work on a new gain-integrated 8×8 silicon switch design. Evanescently coupled SOAs elements and silicon-based T-O MZ switch units are used and assembled in dilated Banyan topology providing a strong suppression. This paper for the first time proposes and assesses the design of a 8×8 gain-integrated silicon switch building block, showing a 0.2dB power penalty floor at 10^{-9} BER and a 17dB IPDR for 1dB penalty. A 64×64 Clos switch is subsequently modelled exhibiting a 0.7dB penalty floor and 10dB IPDR with power penalty less than 1dB.

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