ENABLING HIGH-RESOLUTION FLUORESCENCE IMAGING AND DETECTION USING INTEGRATED PHOTONICS

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Introduction

The ultimate resolution in microscopy is set by the diffraction limit. Various super resolution (SR) techniques have been developed in the recent years to surpass this limit. Among these techniques the one that gained the most traction is structured illumination microscopy (SIM) owing to the following advantages [1]:

- Efficient use of photon budget / least photo-toxic
- Relatively high imaging speed among other SR techniques
- Compatibility with conventional fluorophores used

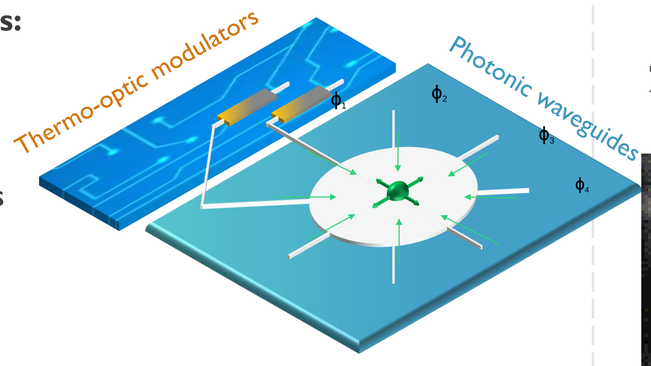
However, all the SR techniques including SIM suffer from common drawbacks: low throughput, bulky and expensive equipment. High throughput imaging excitation can be realized by means of waveguide excitation in a photonics integrated circuit (PIC) chip together with a large field-of-view (FOV) objective. It has recently been demonstrated that high throughput is achieved with such a configuration [2]. PIC can be integrated on top of a CMOS imager as the next step. This is possible by using the plasma enhanced chemical vapor deposition (PE-CVD) developed at imec [3].

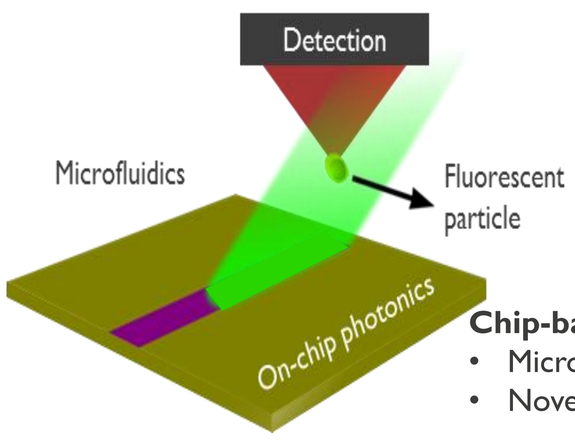
Furthermore, together with integrated microfluidics PICs holds promise for miniaturization of flow cytometry. Sorting cells based on fluorescent labels is an essential step in various research and clinical applications [4, 5].

Here we demonstrate two devices:

SIM PIC chip:

- Cost-effective and portable
- On-chip thermo-optic modulators
- CMOS compatible





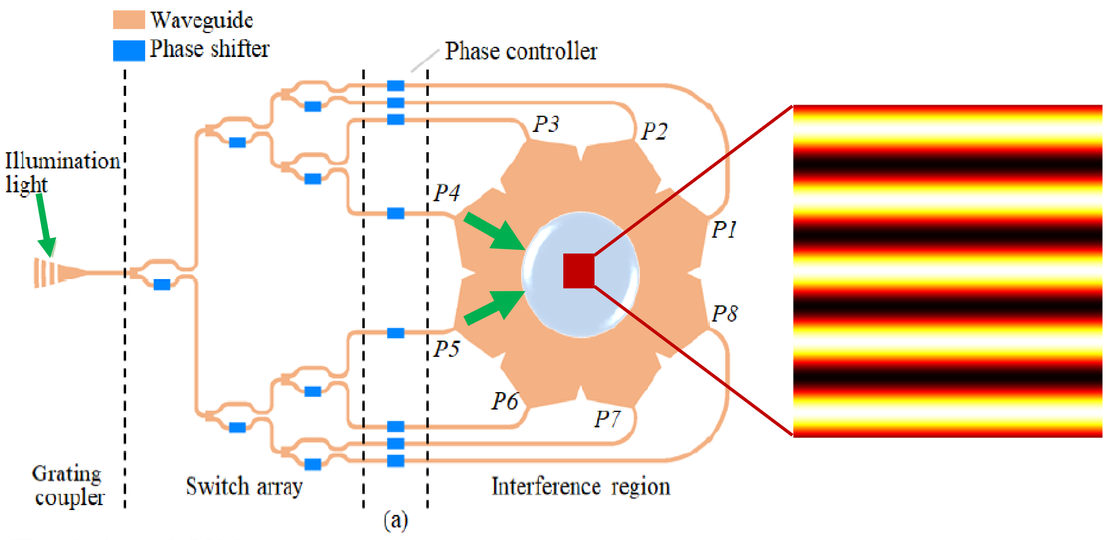
Chip-based flow cytometer:

- Microfluidics integrated on a PIC
- Novel grating design -> uniform illumination

Method

On-chip SIM works as follows:

1. Couple illumination light into the PIC through a grating coupler
2. Tune thermo-optic phase modulators by applying voltage
3. Generate the desired structured illumination pattern
4. Capture raw images looping through steps 2-3
5. Reconstruct super-resolution image



Traditional SIM:

- Illumination and detection through the same microscope objective
- Modulation frequency of the illumination pattern bounded by objective
- Lower number of raw images

On-chip SIM:

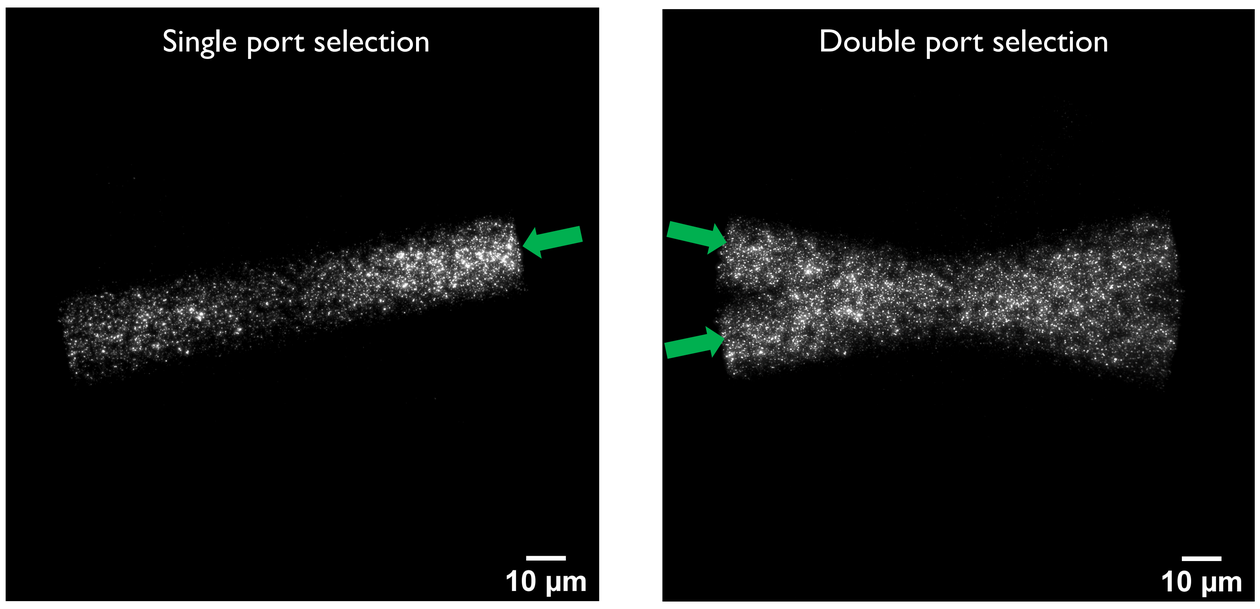
- TIRF illumination through photonic waveguides
- High throughput imaging with a large FOV objective
- Increased number of raw images

References:

1. Heintzmann, R. & Huser, T. Chem. Rev. **117** (2017) 13890–13908.
2. Helle, Ø. I. *et al*. Nature Photonics (2020).
3. A. Z. Subramanian et al., IEEE Photonics Journal **5** (2013) 6.
4. K. de Wijs et al., Lab Chip **17** (2017) 1287-1296.
5. D. Vercruysse et al., Lab Chip **15** (2015) 1123-1132.

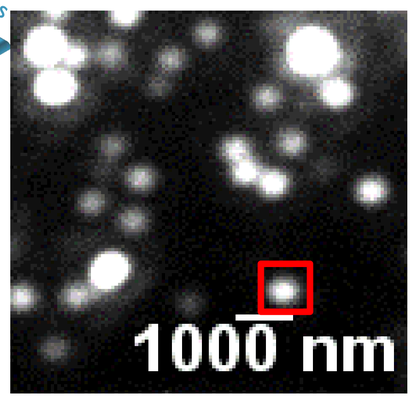
Results of on-chip SIM

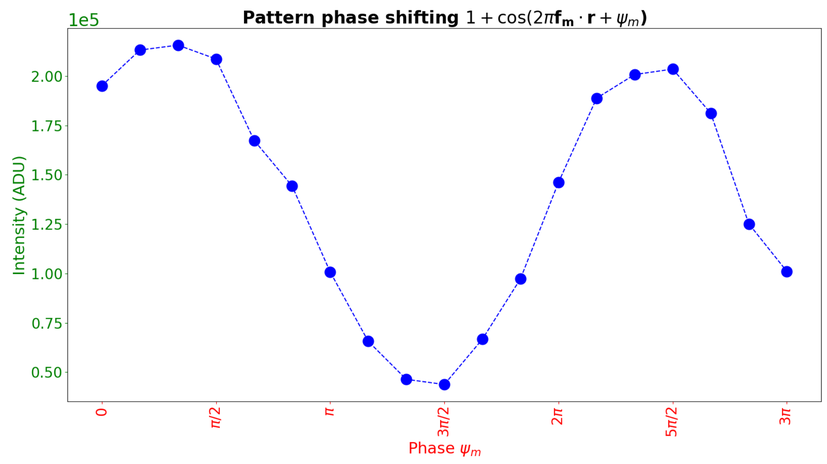
1. Selection of different ports for SI



The imaging area is deposited with 100 nm fluorescent beads. These results confirm that single/multiple ports can be selected with high accuracy via electrical actuation of the thermo-optic modulators.

2. Phase shift of sinusoidal illumination pattern

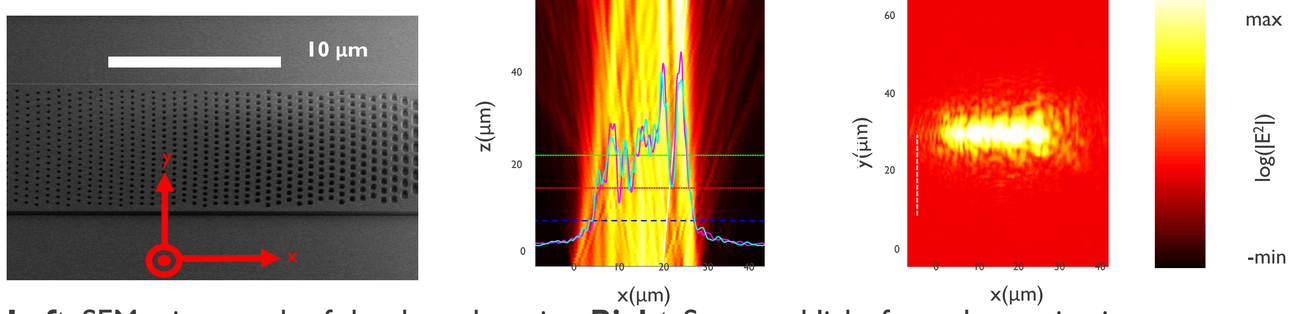




Left: Micrograph of fluorescence emission from 100 nm fluorescent bead clusters, show in red box is the region of interest **Right**: Sweeping the phase of the sinusoidal illumination pattern

Results of chip-based flow cytometer

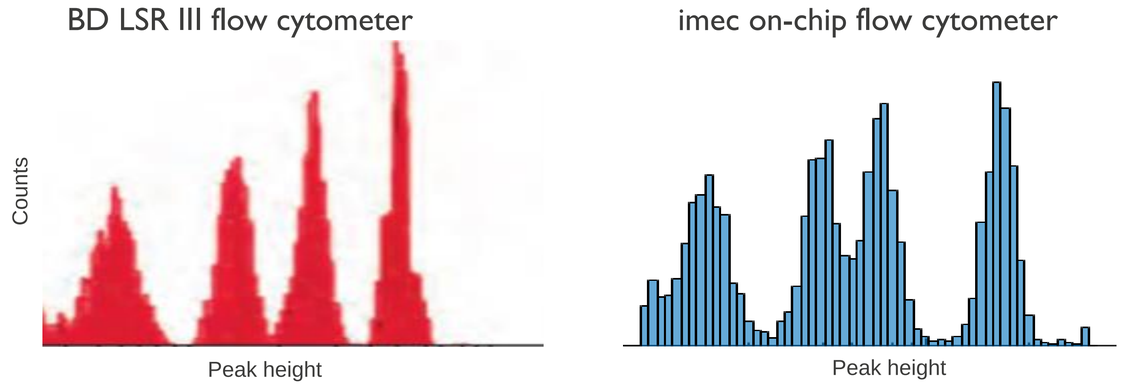
1. Uniform illumination



Left: SEM micrograph of the dotted grating. **Right**: Scattered light from the grating in logarithmic scale.

2. Calibration beads test

Peak height histogram for a mixture of calibration beads with different number of fluorescent markers imitating a cell-sorting scenario.



Conclusion

A portable, PIC based SIM device that generates structured illumination patterns with thermo-optic phase modulators is demonstrated. The same concept can be expanded to achieve other functionality through monolithic integration of PIC chip on a CMOS imager. This also eliminates the need for a host optical setup and alignment. Furthermore, the on-chip flow cytometer achieves uniform illumination and shows comparable sorting performance with commercial cytometers. The device design allows for dense parallelization yielding high throughput.