CMOS Compatible Thermal Management for Silicon Photonic Optical Phased Arrays

A. Krochin[1,2]; Dr. U. Scholz[1] ; Prof. Dr. A. Zimemrmann[2,3]
[1]Robert Bosch GmbH – Advanced Technologies and Micro Systems (CR/ATM)
[2]Institute for Microintegration (IFM) - University of Stuttgart
[3]Hahn-Schickard

Motivation

Silicon photonic **optical phased arrays** (OPAs) are strongly **temperature dependent**:

- **Temperature** fluctuations, gradients and offsets **influence** functionality of **OPAs** [1].
- Novel **thermal management** solutions are **required** to guarantee proper functionality of silicon OPAs [2,3].

Background

- **Optical phased arrays** are **phase sensitive**, solid-state **beam steering devices**

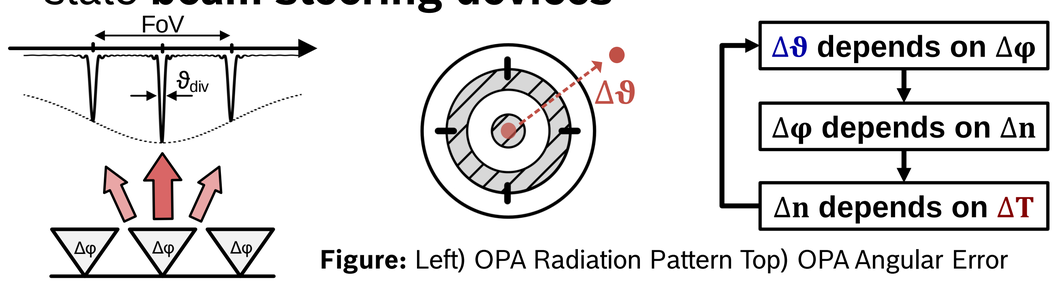


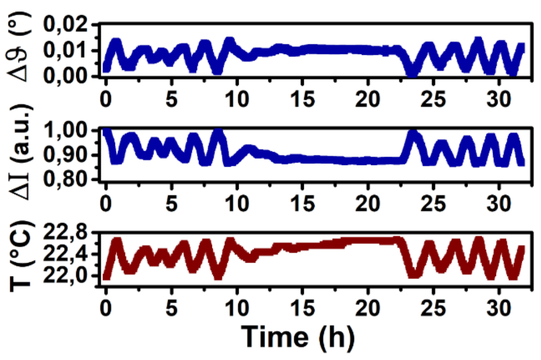
Figure: Left) OPA Radiation Pattern Top) OPA Angular Error

- **Strength** of the temperature influence **depends on** OPA **implementation**[1] and **α depends** on OPA initial **calibration**.

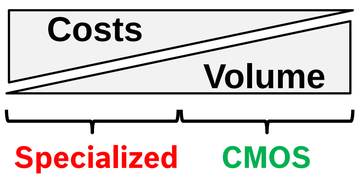
$$\Delta\vartheta \approx \frac{L}{d} \cdot \frac{\partial n}{\partial T} \cdot \Delta T_{diff} + \alpha \cdot \Delta T_{off}$$

L: Component Length
d: Component Pitch
∂n/∂T: Thermo-optic coefficient
α: Offset / Calibration factor

Figure: Response of a prototype OPA towards room temperature fluctuations.



- **CMOS** compatible **thermal management** solutions are **required.**



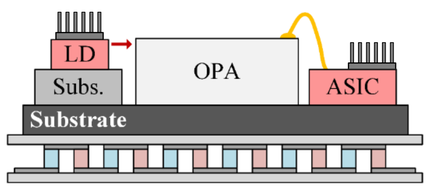


Figure: OPA system with specialized thermal management solutions

Approach

- Perform **structural modifications** within the photonic IC to **change** the preferred **heat paths.**

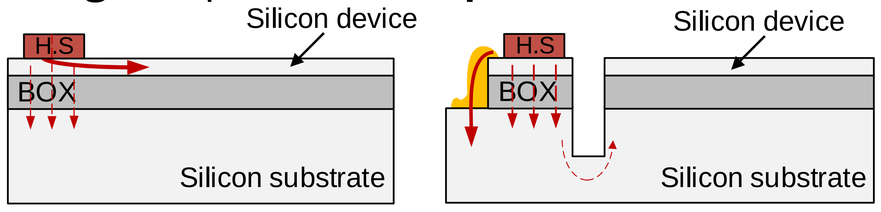


Figure: Left) Conventional Photonic IC. Right) Photonic IC with Heat Shunts and Trenches.

- Alternate **CMOS processes** (e.g. PVD, CVD, IBE, DRIE, Lithography) for **fabrication** of thermal **demonstrators**.

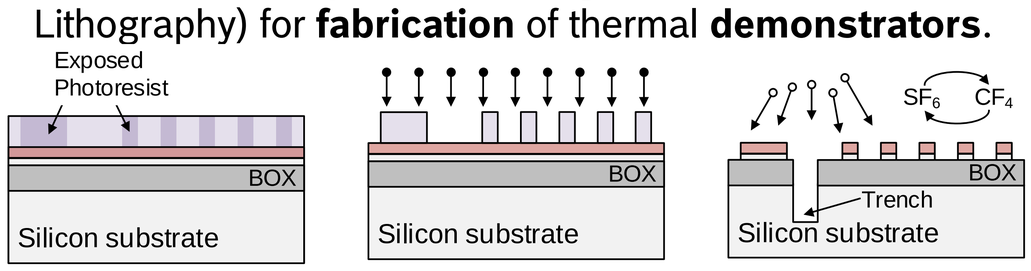


Figure: Left) Lithography Step. Center) IBE Step. Right) DRIE Step.

Results

- **Confirmed** concept **feasibility** by fabrication and characterization of **thermal demonstrators.**

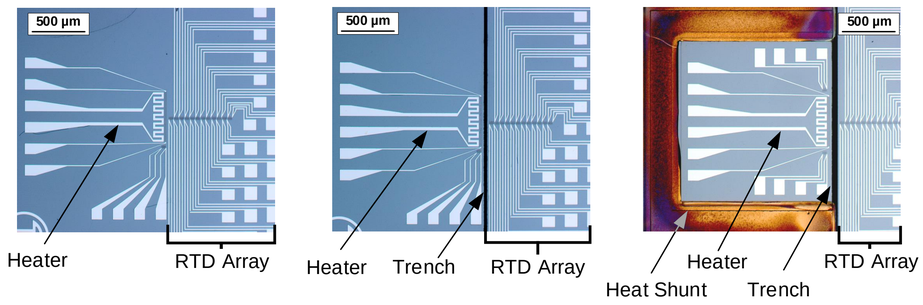


Figure: Left) Reference thermal demonstrator. Center) Thermal demonstrator with trench. Right) Thermal demonstrator with trench and heat shunts. Figure adapted from [2]

- **Trenches reduce safe distances (x_{safe}) at the cost of an increased heat source temperature.**

width → / ↓ depth	Safe distance x_{safe} 25 µm	50 µm	100 µm	Heat source temperature 25 µm	50 µm	100 µm
0 µm		1393 µm			74.7 °C	
119 µm	913 µm	777 µm	768 µm	81.0 °C	88.1 °C	92.7 °C
254 µm	259 µm	273 µm	473 µm	95.3 °C	92.0 °C	96.1 °C
330 µm	217 µm	234 µm	279 µm	103.1 °C	105.0 °C	111.2 °C

Table: Comparison of the calculated safe distance x_{safe} and the heat source temperature for different trench widths and trench depths.

- **Heat shunts** provide a **high thermal conductivity connection** between heat source region and silicon substrate
  → **preferred path** for heat dissipation
  → **reduction of thermal resistance**

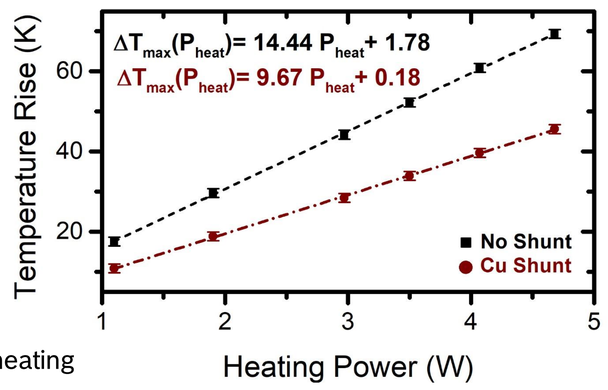


Figure: Temperature rise for different heating powers with and without heat shunts.

- **Combination** of trenches and heat shunts provide a **convenient solution** to **reduce** on-chip temperature **gradients** and **improve** heat **dissipation**

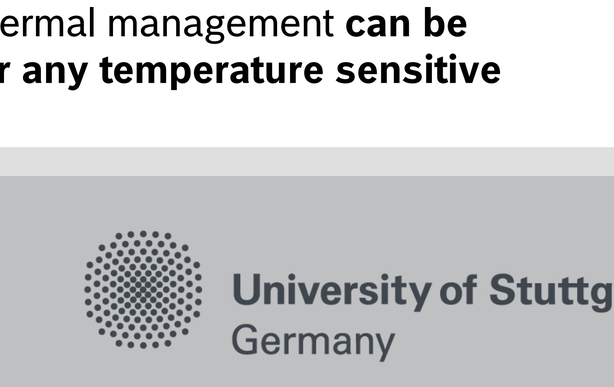


Figure: Temperature profile on thermal demonstrator.

Conclusions

- **CMOS compatible solutions** for thermal management of silicon photonic OPAs were **successfully demonstrated.**
- **Trenches reduce x_{safe}** by over 80 %
  → **Trade-offs** between trench width, depth and reduction of temperature gradients were **identified**.
- **Heat Shunts reduce thermal resistance** by over 30 %.
- **Modular solutions** for thermal management **can be applied** beyond OPAs **for any temperature sensitive photonic IC.**

1: Krochin et al. , IEEE Photonics Journal, Vol. 12 No. 2 (2020)
2: Krochin et al. , MDPI Photonics, Vol. 7 No. 1 (2020)
3: Krochin et al. , IEEE Photonics Journal, Vol. 11 No. 4 (2019)

Contact: Andrei Krochin, Robert Bosch GmbH
PedroAndrei.KrochinYepez@de.bosch.com

University of Stuttgart
Germany