CMOS Compatible Thermal Management Solutions for Silicon Photonic Optical Phased Arrays

Pedro-Andrei Krochin-Yepez[1,2], Ulrike Scholz[1] , Andre Zimmermann[2,3]
[1] Department of Microsystems and Nanotechnologies (CR/ARY), Corporate Sector Research and Advance Engineering, Robert Bosch GmbH, 71272 Renningen, Germany
[2] Institute for Micro Integration (IFM), University of Stuttgart, 70569 Stuttgart, Germany
[3] Hahn-Schickard. 70569 Stuttgart Germany

e-mail: PedroAndrei.KrochinYepez@de.bosch.com

ABSTRACT

Silicon photonic optical phased arrays (OPAs) are promising candidates to become the next generation beam steering systems. However, due to the large thermo-optic coefficient of silicon, their functionality depends strongly on the temperature. Therefore, efficient thermal management solutions, allowing for efficient heat dissipation as well as reduction of on-chip temperature gradients, are required to guarantee the correct functionality of silicon photonic OPAs. Here, two CMOS compatible thermal management solutions are proposed and evaluated. The proposed solutions can be implemented either individually or in combination to address the different thermal management requirements of any particular OPA system.

Keywords: optical phased arrays (OPAs), silicon photonics, photonic thermal management, CMOS.

1. INTRODUCTION

With the advent of optical technologies, optical beam steering systems have become fundamental building blocks required to enable a wide range of future applications, from free-space optical communications to imaging applications. State-of-the-art optical beam steering systems rely on mechanical movement of components, such as mirrors, prisms or lenses. While these mechanical systems allow steering light beams over large fields of view, they are usually slow and bulky. Furthermore, the movable components rise reliability concerns particularly in applications where vibration and shock resistance is required. In such applications, solid-state systems, allowing for beam steering with no movable components, are desired. Due to the missing component inertia, solid-state systems not only eliminate mechanical stability concerns, but also achieve much higher steering velocities, than mechanical beam steering systems [1].

Optical phased arrays are promising system, to enable two dimensional solid-state beam steering. An optical phased array consists of an array of optical emitters, whose phase can be individually modified using optical modulators. Changing the phase of the individual emitters enables beam steering along the ϑ-direction [2]. Furthermore, using grating structures as optical antennas, in combination with widely tuneable laser sources allows beam steering along the ψ-direction. Therefore, the combination of an OPA with grating antennas enables for two-dimensional solid-state beam steering. Silicon photonic OPAs not only leverage from the advances in high-speed optical modulators done by the telecommunications industry, but due to its compatibility with the well-established CMOS fabrication process, large number of OPAs can be fabricated at extremely low costs, making silicon photonic OPAs promising candidates to become the next generation solid-state beam steering system.

Due to the large thermo-optic coefficient of silicon, its refractive index strongly depends on the temperature. Therefore, the functionality of phase sensitive components, such as optical phased arrays, is expected to be particularly sensitive towards temperature [3]. Not only ambient temperature fluctuations, but also temperature offsets due to inefficient heat dissipation and even temperature gradients within the photonic IC, can lead to malfunction of the system. To guarantee the correct functionality of OPA systems, thermal management solutions, allowing not only for temperature stabilization, but also for efficient heat dissipation as well as for reduction of temperature gradients, need to be developed. Furthermore, to comply with the advantages of silicon photonics, the proposed thermal management solutions must allow for low power operation and must be compatible with the CMOS processes used for the fabrication of the photonic ICs [4].

Here, two different CMOS compatible solutions enabling efficient heat dissipation as well as reduction of temperature gradients, without additional power requirements are presented. The first solution consist of using trenches, to decouple the photonic IC in two independent thermal regions, namely the temperature sensitive and the heat source region. Thermally decoupling both regions allows reducing gradients in the temperature sensitive region at the cost of an increase in the temperature of the heat source region. In addition to the use of trenches, the

second solution proposes the use of so-called heat shunts as thermal bridges between the heat source region and the silicon handle layer of the SOI substrate. Fabricating heat shunts with high thermally conductive materials allows improving the heat dissipation of the system and hence reducing the temperature of the heat source region.

2. Trenches for Thermal Decoupling of Photonic ICs

As mentioned above, the first solution proposes the use of trenches to separate the photonic IC in independent thermal regions. The region where heat generating components, such as laser sources and driver electronics are found, is called the heat source region, and the region where phase sensitive components are found, is referred to as the temperature sensitive region. As shown in Figure 1, placing trenches between the heat source region and the temperature sensitive region reduces the thermal cross talk between both regions, reducing hence temperature gradients in the temperature sensitive region.

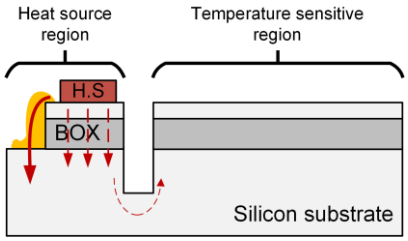

Figure 1. Schematic representation of a silicon photonic IC with trench for thermal separation and heat shunt for efficient heat dissipation. Red arrows represent the heat flow through the photonic IC. Figure adapted from [4].

To quantify the efficiency of trenches in reducing temperature gradients, the concept of safe-distances is used [4]. The safe distance, x_{safe}, is defined as the distance from the heat source at which the temperature rise is smaller than defined temperature increment, ε. As shown in Table 1, the efficiency of the trenches in reducing the safe distance depends on the trench depth, d, as well as on the trench width, w.

TABLE 1. Calculated safe-distances x_{safe} for an un-trenched photonic IC (d=0µm) and for a photonic IC with different trench widths and trench depths, considering a tolerable temperature increment $\varepsilon = 1\ K$. Values obtained from [4].

	$\boldsymbol{w = 25\ \mu m}$	$\boldsymbol{w = 50\ \mu m}$	$\boldsymbol{w = 100\ \mu m}$
$\boldsymbol{d = 0\ \mu m}$	$1392.5 \pm 158.2\ \mu m$		
$\boldsymbol{d = 119\ \mu m}$	$913.2 \pm 258.6\ \mu m$	$777.3 \pm 226.5\ \mu m$	$768.4 \pm 196.6\ \mu m$
$\boldsymbol{d = 254\ \mu m}$	$259.4 \pm 84.6\ \mu m$	$273.1 \pm 105.6\ \mu m$	$473.4 \pm 142.6\ \mu m$
$\boldsymbol{d = 330\ \mu m}$	$217.2 \pm 77.1\ \mu m$	$233.5 \pm 76.8\ \mu m$	$279.3 \pm 68.9\ \mu m$

It was found, that using trenches allows to reduce the safe distance by up to 84 % (from 1392.5 µm to 217.2 µm) in case of a 330 µm deep and 25 µm wide trench. It must be noted that while for small trench depths, the safe distance increases with increasing trench width, for larger trench depths, narrow trenches seem to have a better effect in reducing the safe distances. A possible reason for this behaviour is the increased heat source temperature, leading to larger temperature gradients. One way to reduce the heat source temperature is to create a thermal bridge between the heat source region and the silicon substrate by depositing a material with a higher thermal conductivity than silicon dioxide.

3. Heat Shunts for Efficient Heat Dissipation

Since including trenches reduces the heat dissipation area, it increases the thermal resistance of the system, increasing the temperature of the heat source region. To overcome this drawback, it is proposed to use heat shunts, to create a thermal connection between the heat source region and the silicon substrate of the photonic IC [4].

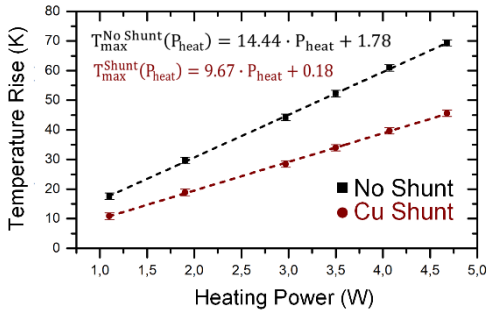

Figure 2. Comparison of the temperature rise for different heating powers between a sample without heat shunts and a sample with a 2.5 µm thick Cu-heat-shunt. Figure adapted from [4].

To quantify the influence of heat shunts of reducing the heat source temperature, the thermal resistance of a system with and without heat shunts is determined. The thermal resistance is obtained by measuring the temperature rise for different heating powers. In Figure 2 it can be seen, that using a 2.5 µm thick Cu-heat shunt allows to reduce the thermal resistance by 33% (from 14.44 K/W to 9.67 K/W).

4. CONCLUSIONS

From the results obtained during these investigations, it is possible to conclude that trenches are an extremely powerful measure to reduce temperature gradients. While it was found that including trenches increased the thermal resistance, leading to an increased heat source temperature, the reduction of temperature gradients outweighs this drawback. Furthermore, it was demonstrated that including heat shunts in addition to the trenches allows to considerably improve the heat dissipation reducing the temperature in the heat source region.

While further investigation are required to determine the best performing combination of trench depth and width, as well as to determine the influence of the heat shunt material and geometry on the heat dissipation, from the current results it can be concluded that in the present form, the proposed solutions help to fulfil the thermal management requirements of temperature sensitive optical phased arrays.

REFERENCES

[1] P.F. McManamon and A. Ataei: Progress and opportunities in optical beam steering, *in Proc. Quantum Sensing and Nano Electronics and Photonics XVI*, *SPIE*, San Francisco, California, 2019.

[2] J. Sun, et.al.: Large-scale nano-photonic phased array, Nature, vol. 493. pp 195-199, 2013.

[3] P.A. Krochin-Yepez, et.al.: Temperature Dependence of the Steering Angles of a Silicon Photonic Optical Phased Array, *IEEE Photonics Journal*, (Early Access), 2020.

[4] P.A. Krochin-Yepez, *et al.*: CMOS-Compatible Measures for Thermal Management of Phase-Sensitive Silicon Photonic Systems, *Photonics*, vol. 7, issue 1, 2020.