Fabrication of Silicon Nitride PIC by Laser Direct Writing

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ABSTRACT

We report our first results in the fabrication of photonic integrated circuits in silicon nitride platform by laser direct writing. These are novel and preliminary results in the area of micro-fabrication of photonic integrated circuits in Argentina and the Latin-American region. We were able to demonstrate the feasibility to carry out a maskless high-resolution lithography via a low cost process.

Keywords: photonics, silicon nitride platform, direct writing laser, photolithography, micro-fabrication.

1. INTRODUCTION

Ultra-violet (UV) laser direct-writing (LDW) lithography is a technique that enables to transfer patterns directly over the photoresist (PR) without the need of a physical mask (maskless lithography). The main advantage of LDW is the possibility of obtaining high resolution (submicrometer) inscription of a pattern by means of an inexpensive procedure. While electron beam lithography (EBL) technique can reach finer resolutions in comparison to LDW, the cost of implementing EBL is higher. However, regarding silicon nitride (SiN)-based photonic integrated circuits (PICs), the required waveguide sizes and gaps can be accurately defined employing the LDW technique, and several designs have been recently reported [1,2]. Maskless lithography also provide an alternative for rapid PIC prototype fabrication without the mask manufacturing extra cost of standard lithography [3].

In this manuscript we present our first results of UV LDW waveguide designs written in a silicon nitride platform. The general outline of this project is to explore the feasibility of developing a standard procedure for UV LDW of photonic waveguides in a SiN platform using the cleanroom facilities of CNEA (Comisión Nacional de Energía Atómica). The possibility of rapidly fabricating PIC prototypes at CNEA facilities unlock a list of new opportunities for researchers, technicians and photonics start-up companies from Argentina and the region, to implement their designs. To our knowledge this is the first institution in Latin-America that is able to offer such kind of service.

2. FABRICATION

Following are presented the different steps for the fabrication process of a calibration layout and the implemented prototypes:

2.1 Wafers

The wafers are composed of three-layers: a silicon substrate, a buried layer of SiO_2, and a top layer of SiN. They were fabricated in the laboratory according to the following steps:

- First, the wafers were cleaned with hydrogen fluoride (HF) to remove native silicon dioxide.
- Then, a 440 nm layer of SiO_2 was grown by using dry thermal oxidation.
- Finally, the layer of silicon nitride was deposited using PECVD technique with SiH_4 (2%) and NH_3 as reactive gases, adjusting the recipe for 300 nm deposition.

A Horiba AUTO/SE ellipsometer was used to measure the thickness of the SiO_2 and SiN films over forty-nine points around the entire wafer surface. A 5 nm thickness standard deviation was obtained for both layers.

2.2 Lithography

The photoresist (PR) was exposed employing UV light commercial equipment which has a laser diode operating at 405 nm for direct writing. A 2 mm focal length head lens was used to focus the laser beam on the sample surface to obtain submicrometer resolution.

The stage system is equipped with a motor having X-Y motion controlled by interferometry, and a vacuum chuck where the sample is located. The shutter and the displacement of the sample are controlled by the system

computer. The user can set the energy of the laser during exposure (set in terms of the percentage of the maximum energy) and the focus deviation (DeFOC) from the default lens position.

In the laboratory, this laser system is typically employed to manufacture masks for standard lithography applications, nevertheless, it can be used for LDW on wafers up to 4’’. Positive photoresist AZ 1518, which is typically used in commercial metallized plates, was used for simplicity and expense reduction. The wafer was coated, first with an adhesion promoter from TI-Prime, and after that with the PR diluted in solvent (4:3) in order to reach approximately 530 nm of thickness at 4000 rpm.

In order to set the calibration parameters used for exposure of the direct lithography process, it was used a layout with vertical and horizontal lines with gap and width values, both varying from 600 nm to 1200 nm. Figure 1(a) shows a section of the calibration layout. These structures were exposed repeatedly in a structure with a matrix shape over the wafer with different parameters of energy and DeFOC. After the exposition, the photoresist was developed with AZ 351B in a 1:3 dilution of deionized (DI) water. Figure 2(b) shows an optical micrograph of the calibration structures after the lithography process.

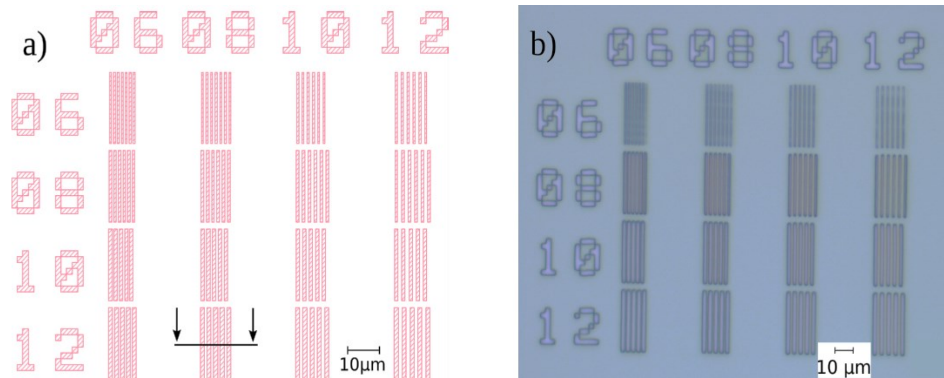

Figure 1: Calibration structures. (a) Layout in GDSII format (vertical lines). The black line with arrows corresponds to the SEM cut illustrated in Fig. 2. (b) Vertical lines after exposing and developing the PR.

2.3 Etching

In order to perform the SiN etching process, an Oxford Plasmalab 80plus reactive-ion etching (RIE) equipment was used, using sulfur hexafluoride (SF_6) as the reactive gas. With such configuration we were able to obtain an attack rate of 4.5 nm/s. The samples were etched for 90 seconds. Once the process was finished, a Quanta 3D 200i scanning electron microscope (SEM) with a high current focused ion beam (FIB) was used to observe the resultant structures.

3. RESULTS AND DISCUSSIONS

The line patterns were measured by an analysis performed over the SEM images. Figure 2(a) shows one case where the designed lines have a width of 1200 nm and are separated by 800 nm gaps. The cross-section of the guides and the three layers stack, plus the PR is illustrated in Fig. 2(b).

The fabricated waveguide has trapezoidal section with an angle of $(80 \pm 3)°$ measured from the horizontal surface. Regarding the width, there is a difference between the designed and obtained features. At the waveguide base, the width is approximately 50 nm less than the design value, while at the top the difference increases to 200 nm. These inaccuracies become the opposite when the gap values between waveguides are considered. This discrepancy in the sizes arises from the lithography process where the structure is defined on PR. Particularly, the positive photoresist increases the width of waveguides while reducing the separation between them. This effect can be compensated using a spot correction when the digital designs are transferred to the equipment.

One another note, it was possible to check the selectivity of the RIE attack between the PR and SiN. Figure 2(b) shows the remaining PR layer over the structures. It can be seen that has a thickness value that approaches150 nm, while the unprotected silicon nitride was fully etched by the plasma.

The obtained results in the calibration were used to set up the exposition parameters in the LDW (energy, DeFOC and spot correction). Finally, photonic circuits were designed and fabricated using the three-layer wafer method already described, following the same steps detailed for the calibration procedure. The implemented designs primarily consist of three type of structures: waveguides for propagation and bend losses characterization, and power splitters. Figure 3 shows an optical micrograph of a fabricated Y-branch splitter. The waveguide was designed with a width of 1500 nm for single-mode operation at a wavelength of 1.55 µm.

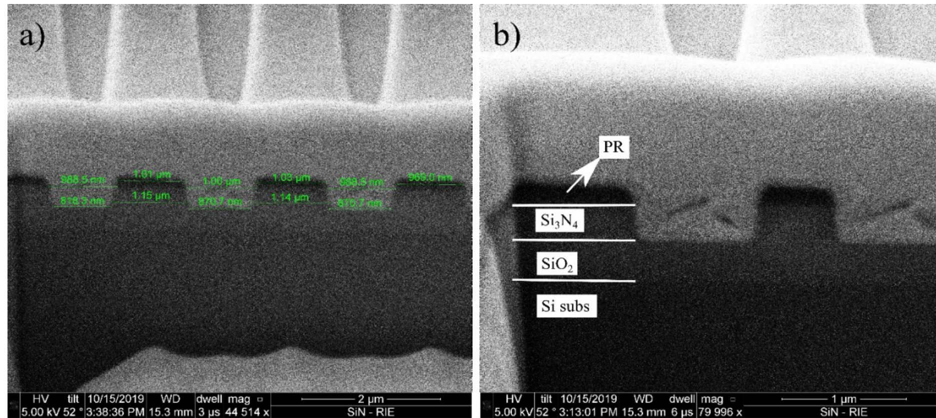

Figure 2: SEM images of the fabricated silicon nitride structures. (a) Designed lines of 1.2um separated by 800nm. (b) Cross-section of the waveguides and the three layers stack plus PR.

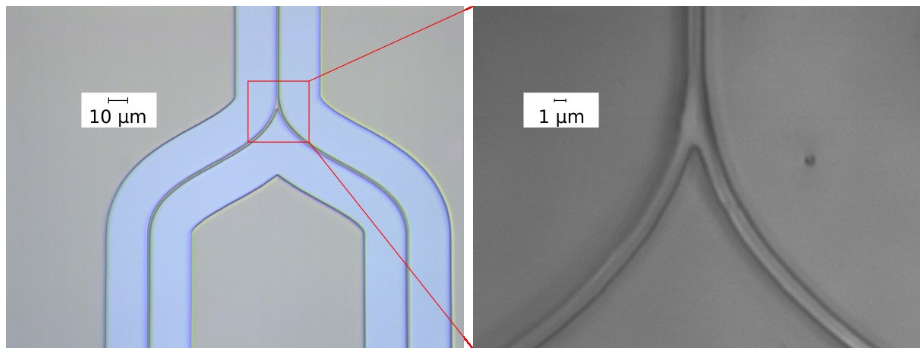

Figure 3: Optical micrograph of the fabricated Y-branch splitter base on silicon nitride platform. The inset shows an optical zoom of the split zone.

4. CONCLUSIONS

We presented a manufacturing procedure and fabrication results of UV laser direct-writing photonic waveguides in SiN platform, achieving submicrometer resolution. Particularly, a power splitter was shown with a clean and well defined pattern, having dimensions according to the expected values that the fabrication method allows. In addition, the obtained fabrication tolerances can be reduced by a proper adjustment of the parameters during the lithography, i.e. energy, DeFOC and spot correction values. The minimum feature size that can be reached with this technology of fabrication approaches 800 nm, which is enough for most of the applications employing SiN technology. However, we are still redefining the fabrication processes (mainly with the plasma attack) to improve the rectangular shape of the waveguide section.

The presented results demonstrate the possibility of fabricating PICs based on silicon nitride platform by UV LDW lithography within the CNEA facilities. Maskless lithography is a very important tool to reduce the cost of prototyping circuits and speed up the time between design, fabrication and testing (one of the most common problems for research in Argentina).

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