Silicon nitride passive photonic platform for applications at visible wavelengths: design, fabrication and characterization

(Student Paper)

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ABSTRACT

Silicon nitride (Si_3N_4) is a material of choice for development of versatile photonic platform due to its wide transparency window ranging from visible to mid-infrared range, CMOS-compatibility, low loss and compactness of the devices. In this paper, we report recent results of development of Si_3N_4-based photonic devices as an initial step to establish flexible generic technology photonic platform and to offer multi-project wafer (MPW) production runs. Three sets of test devices have been developed: waveguides (WGs) including tapers and bends, symmetrical multimode interferometer (MMIs) couplers and arrayed waveguide gratings (AWGs). Obtained results confirms robustness of the Si_3N_4 material platform. Average measured losses in WGs at 660 nm of 1.7 ± 0.5 dB/cm have been achieved with average single 90° bend loss of 0.22 ± 0.01 dB for 100 μm bending radius. MMIs 1×2 show average losses of 0.49 ± 0.05 dB and MMIs 1×4 of 5.53 ± 0.43 dB. Measured AWGs 1×8 free spectral range and channel spacing match design values.

Keywords: silicon nitride, photonic integrated circuits, biophotonics, silicon photonics, arrayed waveguide grating, generic technology

1. INTRODUCTION

Recent pursuit in replacing electronic devices with photonic integrated circuits in a growing number of applications resulted in a need for a silicon-compatible, broadband, compact, economically and technologically achievable platform with a potential for cross-platform monolithic / hybrid and opto-electronic integration [1]. Aside from silicon on insulator (SOI) and indium phosphide (InP) a silicon nitride completed the triad of commercial platforms. Si_3N_4 wide transparency window, low thermo-optic coefficient, perfect technological and economical match for integration with CMOS electronics predispose this platform for above applications and cross-platform integration by means of molecular or adhesive wafer bonding. Si_3N_4 as a third commercial-level platform in comparison to its competitors InP and SOI, offers lower loss waveguides and a higher flexibility in tuning of design parameters for desired applications. Extreme flexibility makes Si_3N_4 a material of choice for biophotonics, telecom, datacom and sensing applications, often as a part of hybrid photonic devices [2].

Several commercial Si_3N_4-based photonic platforms are on various stages of development. The motivation behind the reported work was, however, to investigate the capability of efficient development of domestic photonic platform on existing silicon manufacturing line and without external hand-on expertise. Multimode interferometer (MMIs) couplers and other fixed wavelengths devices designs have been optimized for 660 nm operation and arrayed waveguide gratings (AWGs) have been optimized for operation in wide band range from 570 to 630 nm. Choice of MMIs and AWGs have been contradictory motivated as in case of MMIs, development has been conducted to test robust device in scope of possible manufacture imperfections and in case of AWGs, to test device sensitive to design and manufacture flows.

2. SIMULATION AND DESIGN

Numerical methods implemented in commercial software packages have been utilized for waveguides (WGs) cross-section optimization and later for devices simulations. Film Mode-Matching (FMM) method has been used for investigation of electromagnetic field distribution for modes in WGs and bends. For MMIs and AWGs simulations, a Finite Difference (FD) method has been used. Based on simulation results, WGs test structures of width from 0.3 μm to 2.9 μm have been put into PICs. Delay lines of different cross-sections and bend radiuses were also included. Three topographies were designed. As an example, GDS file and corresponding microscopic image of first designed photonic integrated circuit (PIC) is presented in Fig. 1.

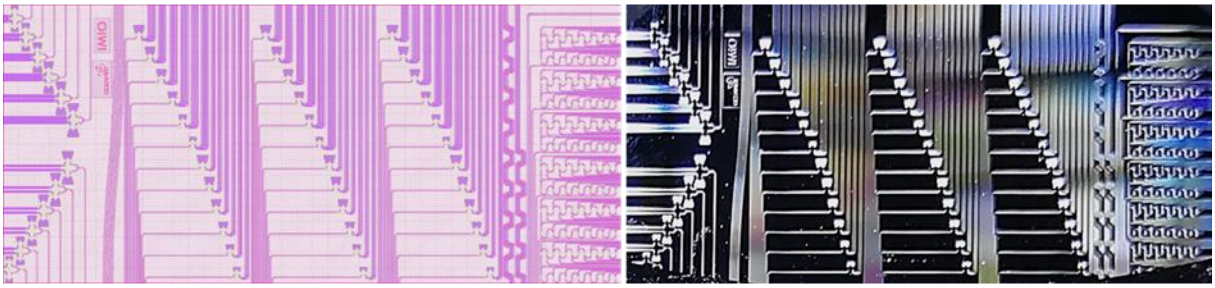

Figure 1. GDS comprising designed test structures (left) and microscopic image of fabricated chip (right).

Exemplary design parameters of MMIs and AWGs are presented in Table 1. All input sections of MMIs are straight WGs, for MMIs 1×4 and 1×8 the output sections are tapered to provide better signal transmission and equal power at each output. Additionally, MMIs 1×4 output section comprises an extra s-bend section to separate closely placed outputs. AWGs are designed with tapered WGs at I/O apertures and image planes for lower loss. The design value of the AWG channel spacing is 0.8 nm (100 GHz). Chosen design parameters for exemplary AWGs are presented in Table 2.

TABLE 1. MMIS GEOMETRICAL DESIGN PARAMETERS

MMI type	λ [nm]	MMR W×L [μm]	Output WGs [μm]	Output WGs offset [μm]	T total	T one output (TE1)
1×2	660	5.5 × 45.0	str.[a] 10.0	±1.35	0.957	0.4785
1×4	660	4.85 × 17.5	str. 10.0 + sb. 10.0×4.5/1.8	±1.80; ±4.50	0.962	0.1400
1×8	660	14.0 × 72.0	tap. 30×1.2/1.0 + str. 30.0	±0.9;±2.7;±4.4;±6.3	0.720	0.0880

[a]str -straight WG, tap – tapered WG, sb – s-bend WG, T - transmission

TABLE 2. AWGS DESIGN PARAMETERS

N×M[a]	λc [nm]	NWGs	RwlR	Order	WgSpac FPR [μm]	Plength [μm]	Olength [μm]	Wc	Op	FSR [nm]
1×8	590	34	45	52	1.4	679.30	1231.65	0.421	0.997	9.551
1×8	610	34	45	54	1.3	728.32	1202.32	0.100	0.998	9.811

[a]AWG N×M – I/O numbers, λc – central wavelength, RwlR – Rowland radius, Order of the array, WgSpac – design waveguide spacing in the array, Plength – physical pathlength of the device between transition waveguide tapers, Olength – optical length of the device, Wc – worst coupling between array waveguides, Op - between straight mode 1 used for the AWG layout with corresponding bend mode, FSR – Free Spectral Range

Python-based scripting environment has been used for building blocks (BBS) and PICs design and generation of GDS files. Hierarchical logic of chosen software environment enabled fast PICs topology generation with multiple-element sections. A library comprising BBs and functional sections has been created and it is to be reused in future development and extended with additional elements.

3. FABRICATION

For all processes, 4’’ silicon wafers (100) were used. After preparatory cleaning process, oxidation in 1200°C was performed creating a 2.3 μm thick SiO_2 layer which serves as a basic separation of waveguide layer and the substrate. The Low Pressure Chemical Vapor Deposition (LPCVD) method was then used to deposit the silicon nitride layer resulting in a layer thickness of 0.32 ± 0.02 μm. Electron beam lithography has been used with a positive resist to pattern the surface accordingly with the designed PICs resulting in an excellent geometrical quality of the structures despite high time consumption of the process. Development of the structures and dry reactive ion etching (RIE) processes followed. The top cladding of 2.3 μm thick SiO_2 was finally deposited in Plasma Enhanced Chemical Vapor Deposition (PECVD) process. SEM images illustrating the quality of manufactured structures are presented in Fig. 2. After processing, wafers have been cleaved into dies as one presented in Fig. 1. Dicing proved to be simple, however, sufficient method of separation for lab characterization.

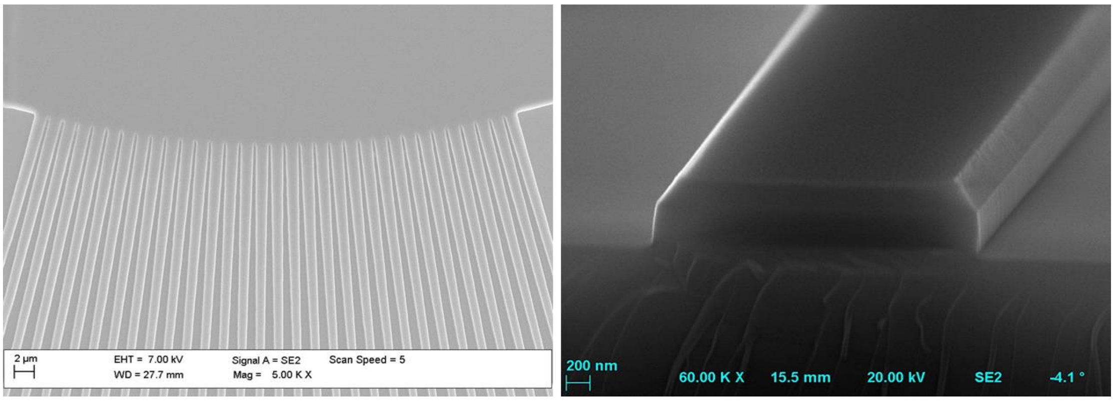

Figure 2. SEM images: output aperture of the AWG (left), WG cross-section before removing resist mask (right).

4. CHARACTERIZATION RESULTS

Measurements of WGs and MMIs have been carried out for 660 nm fixed wavelength with a laser diode and fibre-to-chip edge coupling for input and output. Average measured losses in multimode WGs at 660 nm of 1.7 ± 0.5 dB/cm have been achieved with average single 90° bend loss of 0.22 ± 0.01 dB for 100 µm bending radius. MMIs 1×2 show average losses of 0.49 ± 0.5 dB and MMIs 1×4 of 5.53 ± 0.43 dB. To illustrate robustness of MMI structure in means of wavelength dependent performance, MMIs 1×4 optimized for 610 nm wavelength operation shows additional average 3.79 dB loss while operating at 660 nm AWGs 1×8 performance analysis is presented for AWGs presented in Table 2.

Measurements show moderate offsets of the central wavelength equal 2.85 nm for AWG 1×8 λ_c = 610 nm and 1.67 nm for AWG 1×8 λ_c = 590 nm. This effect is identified as a result of a mismatch between designed and fabricated WGs width and real effective index difference with respect to value assumed in simulations. Other measured AWGs parameters like FSR and channel spacing match the design values up to the measurement accuracy. Comparison of simulated and measured spectra for AWG 1×8 λ_c = 590 nm is presented below in Fig. 3.

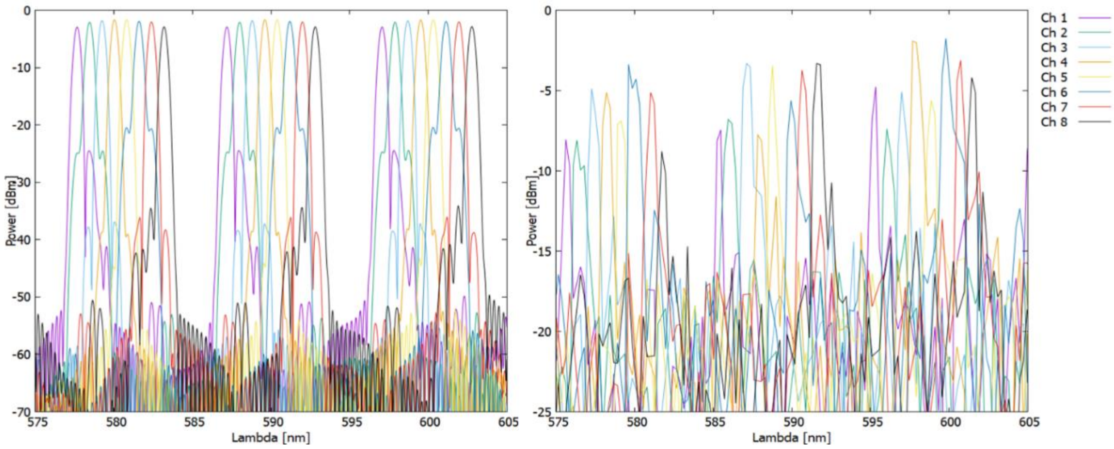

Figure 3. Output spectrum of AWG 100GHz 1×8 λ_c = 590 nm: simulated (left), measured (right).

5. CONCLUSIONS

Working devices of all designed types have been developed within a single production run. This work proves that current state of knowledge, available simulation and design tools merged with operational semiconductor production line enables fast initialization of photonic platform development.

Based on conclusions from an experimental technology run, far-reaching optimization and standardization of design, manufacturing and characterization process have been implemented. Additional steps such double etch depth, metallization for heaters and suspended structures development have been scheduled. Investigation of telecommunication band is planned to verify platform operational band scalability difficulty.

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