Optimized low-loss integrated photonics silicon-nitride Y-branch splitter

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ABSTRACT

Losses is the main detrimental factor that limits the scale of quantum photonic information processing circuits at which they can implement quantum algorithms effectively. Here, we have designed a compact and low-loss Y-branch integrated photonic element for silicon-nitride waveguide. By finite difference time-domain (FDTD) numerical simulation, we have obtained the optimized geometry of the element with loss level of < 0.1 dB at the target wavelength of 808 nm.

1 INTRODUCTION

In the recent years, there has been appreciable interest to integrated photonics as a means of implementation of classical and quantum information processing algorithms. Integrated photonics offers highly stable and miniature realizations of sophisticated algorithms, leveraging the mature CMOS fabrication technologies, thus, providing scaling both in terms of scheme complexity and fabrication volume. For example, integrated interferometer devices, that are capable of performing arbitrary multiport linear transformations are exploited as mode unscramblers [1] or they can be a part of photonic neural networks [9, 3]. In the quantum domain, integrated photonics schemes are indispensible as well. In particular, multi-channel interferometers are a necessary part of the promising quantum computing platform that leverages linear-optical circuits and non-classical properties of photons to realize quantum algorithms [2, 7, 10].

Until recently, the integrated photonic elements were designed by approaches that did not use the full potential of the available fabrication methods, as the basic lithography technology enables delicate manipulation of optical fields on the nano-meter spatial scale. In the recent works, optimization has been applied to design integrated photonic elements with required combination of functionalities, such as small footprint, spectral operation range and polarization characteristics, that are challenging to achieve by the conventional design paradigm [5, 8, 11]. In addition, a variety of specific numerical optimization algorithms have been developed, which are currently a part of specific software packages. This fact made it possible to use the numerical optimization methods by the broad community of researchers.

Most of the previous works on optimization of integrated photonics elements dealt with silicon-on-insulator (SOI) circuits. However, in the past few years the silicon-nitride material platform has been gaining importance, because of the wide wavelength operation range that span from the visible to mid-IR spectral regions, and the absence of two-photon absorption in the telecommunication rang, lacking in the conventional silicon photonics. In quantum photonics in particular, the silicon-nitride platform is beneficial due to the availability of efficient single-photon sources and detectors in the visible region.

Losses is the major detrimental factor limiting the complexity of the quantum algorithms one can effectively implement by optical schemes. The Y-splitter is among the most basic elements that can be used in both classical and quantum integrated optical circuits as a splitter or as a part of two-port modulator interferometers [4]. In this work, we optimize the Y-splitter silicon-nitride element to obtain geometry corresponding to low-loss operation at the target wavelength of 808 nm corresponding to the range of effective single photon sources and detectors. For this purpose, we adopted approach used previously for low-loss silicon-on-insulator Y-splitters [13].

2 DESIGN OF THE Y-BRANCH SPLITTER

We aimed at designing the element of Y-branch splitter, which is supposed to be a part of integrated photonic circuits manufactured by the electron beam lithigraphy. In our simulations the thickness of the silicon-nitride layer was 142 nm — the exact value dictated by the wafer at hand in our fabrication facility. The waveguide width w_0 were chosen to be 600 nm to correspond to single-mode operation at 808 nm wavelength. Fig. 1a illustrates the cross section of a single waveguide with the geometry parameters and materials that are relevant for conducted numerical simulation.

To compare the performance of the Y-branch splitter of our design with analogues, we considered the known design described in [12], which is illustrated Fig. 2a with the superimposed field distribution. This simple design exploits interference implemented in a rectangular region. To alleviate the losses, tapers are added to the design. We optimized the geometry of the rectangular region (its width and length) to obtain as low losses as possible in this design. For this purpose, the FDTD numerical algorithm implemented in the Lumerical FDTD package

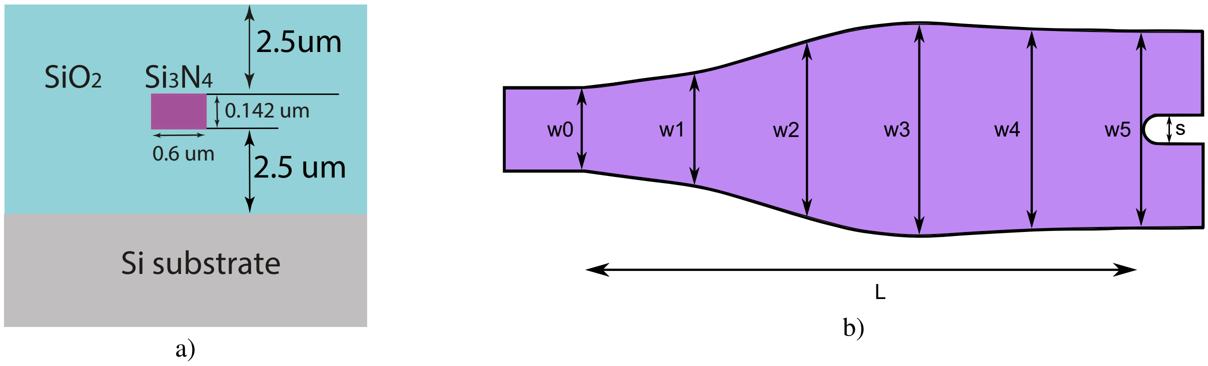

Figure 1. a) Cross-section of a single-mode waveguide with geometry parameters and materials relevant for the FDTD simulation; b) parametrized geometry of the multisection Y-branch splitter, where w_j is the width of section with index j, L is the length of the whole interference region, s is the distance between the inner walls of the output waveguides.

were used to simulate field distribution in the structures. As per optimization, the Particle Swarm Optimization (PSO) method has been used [6], which is a part of the Lumerical FDTD package. As a result, the parameter area was selected so that the structure had the smallest dimensions and minimum loss of 0.18 dB at the target wavelength 808 nm.

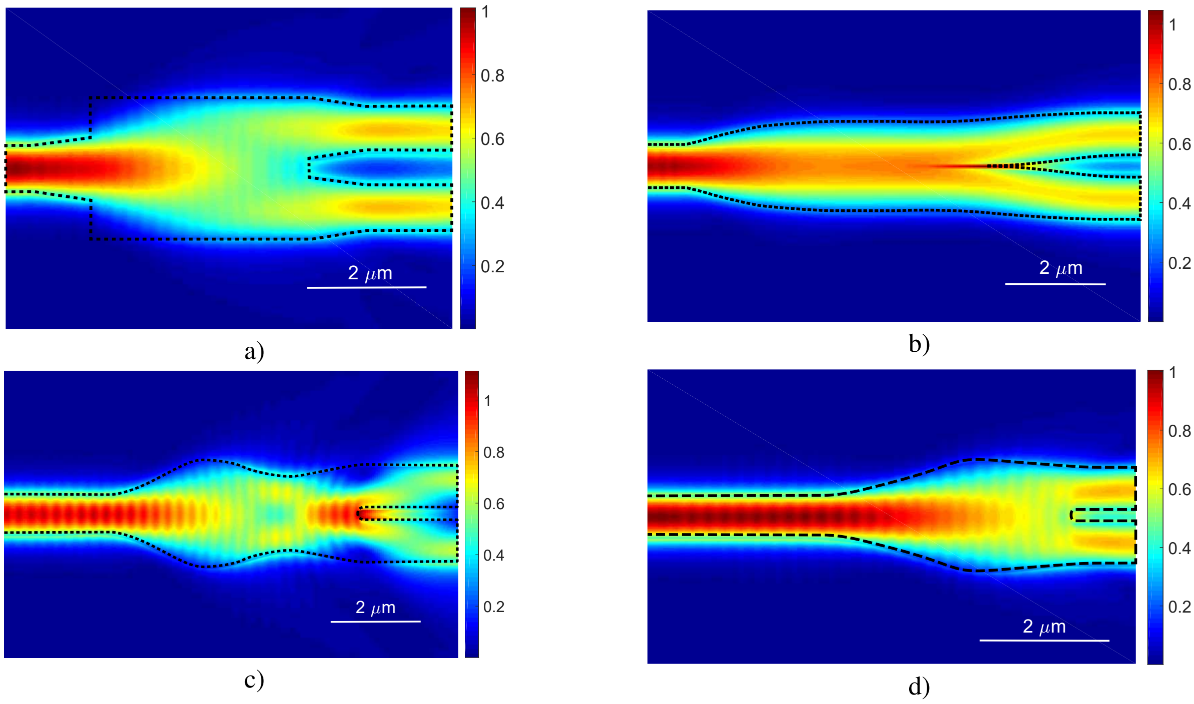

Figure 2. Field distribution in the Y-branch splitters of different designs and geometry parameters: a) simple design with a rectangular interference region and tapers (0.18 dB loss), b) optimized multisection splitter with $s = 0$ (0.1 dB loss), c) non-optimized multisection splitter with $s = 150$ nm (3.3 dB loss), d) optimized multisection splitter with $s = 150$ nm (0.09 dB loss). The corresponding structure geometries are superimposed to the field distribution.

TABLE 1. LOSS LEVEL IN THE OPTIMIZED Y-BRANCH SPLITTERS AT DIFFERENT SECTION NUMBER N AND THE INTER-WAVEGUIDE DISTANCE s.

Number of sections	gap 150 nm, Loss (dB)	gap 200 nm, Loss [dB]
4	0. 119	0.204
5	0.086	0.165
6	0.321	0.249
7	0.09	0.165
8	0.133	0.183
9	0.193	0.226
10	0.114	0.178

We now turn to the approach adopted from [13]. Following this approach, the entire section of a splitter is divided into N section of equal length and different widths w_j, as shown in Fig. 1b. At given N and L

TABLE 2. OPTIMAL DESIGN PARAMETERS OF Y-BRANCH SPLITTER AT $N = 5$, $s = 150$ NM.

w_1 (μm)	w_2 (μm)	w_3 (μm)	w_4 (μm)	w_5 (μm)	L (μm)
0.6	0.815	1.5	1.7	1.35	6.02

optimization proceeds by choosing different values of w_j. The partition of interferometer region into $N = 4 - 10$ section was considered one by one, and for each case the optimal structure parameters have been found that minimize losses with the aforementioned PSO method. Table 1 presents the optimization results for a different number of sections for two different distances s between the output waveguides. The design with 5 sections turned out to be the optimal one, as it provides the smallest losses and its outlines are quite smooth and without unnecessary "tubercles". In Fig. 2 b) shows an optimized structure that does not initially have a gap between the output waveguides. In this case, the loss is 0.1 dB, but this structure is difficult to fabricate due to the presence of an acute angle between the emerging waveguides and a small distance at first between them. The distance between the output waveguides s was limited from below to a value of 150 nm, the limit that sets the chip manufacturing process. For this reason, we have optimized a beam splitter that has a small gap between the output waveguides. In Fig. 2 c) and d) field distribution is shown in non-optimized and optimized designs. Parameters of the divider shown in Fig.2 d) presented in the Table 2.

3 CONCLUSION

We have optimized Y-branch splitter designs to devise the element with as low losses as possible. We have found that the design with 5 sections is enough to achieve optimal low-loss geometry that is possible for the wavelength and the wafer thickness under consideration.

In this work we have demonstrated that optimization methods provides a viable way of decreasing losses in the integrated photonic circuits, which is one of the major detrimental factors in quantum photonics.

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