Compact InP Wavelength Blocker based on a Single AWG and SOA gates for Metro Networks

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ABSTRACT

We present a novel wavelength blocker (WBL) design with a folded configuration for a modular wavelength selective switch (WSS) within the metro network. The folded design enhances scalability of the WSS due its compactness and modularity. The design is experimentally verified with four channels WBL made of a single AWG, SOA-based gates and 90º-waveguide crossing of low loss and low cross-talk (< -65dB). Experimental results show error-free operation with < 1.3dB penalty at 10Gbps NRZ-data.

Keywords: WSS (wavelength selective switch), WBL (wavelength blocker), PIC (photonic integrated circuit).

1. INTRODUCTION

Current state of the art metro networks are quite static and present limited flexibility and scalability. The main drive to enable network flexibility and capacity agility within metro network can be addressed via the implementation of photonic switching nodes while complying with the cost and efficiency requirements of the network. In this regard, the reconfigurable optical add/drop multiplexers (ROADMs) are key elements since they route signals directly in the optical domain as per user requirement. We proposed the implementation of such photonic switching nodes with N-degree ROADM functionality at the metro-core which is constituted by wavelength selective switches (WSS) and 2-degree ROADM based on Wavelength blocker (WBL) at the metro-access networks [1]. On the other hand, the use of photonic integrated circuits (PICs) to realize the WBL is crucial to achieve compact and low-cost large channel count operation. Recently, 8×8 wavelength cross-connect [2] and 4×16 wavelength cross-connect switches [3] have been realized. In a *broad-cast-select* topology, WSS is implemented in a modular fashion, where a single WBL is used per each output port of the WSS. Typically, the implementation of the WBL employs two AWGs and switching gates in between [1-4]. The first AWG de-multiplexes the channels, which can be selectively blocked by the optical gates. The second AWG is then used as multiplexer as illustrated in Fig.1 (a).

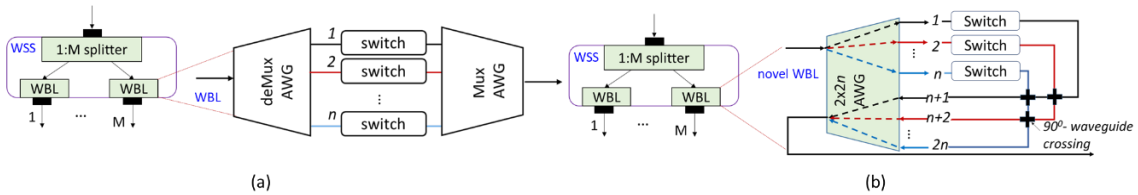

Figure 1. Schematic of *n*-channel *1xM* WSS (a) conventional WBL design (b) proposed WBL design

More compact design can be made by using a single AWG (to be used as both de-Multiplexer and multiplexer) in a folded configuration. This also removes the undesired central wavelength mismatch that happens between the de-Multiplexing and multiplexing AWGs as a result of fabrication error and reduces the number of AWGs by half. Previous works on folded WBL based on Silicon Photonics have been reported in [5, 6]. However, the insertion loss and the cross-talk limit the scalability of those devices. Exploiting SOAs in InP technology to realize the WBL can compensate for the insertion losses and provide high contrast ratio to decrease the cross-talk [3, 4]. A folded configuration employing a single AWG and SOA based optical gates has been also demonstrated in [7]. The main drawback of this work is that the design is based on a single input/output port and hence an external circulator is needed. The lack of a photonic integrated optical circulator prevents the co-integration of the WBL within a more complex PICs. In this paper, we demonstrate a novel folded WBL based on a single 2x2*n* AWG with *n* switches (SOA gates) and low cross-talk 90º-waveguide crossing for switching of *n* WDM channels as illustrated in Fig.1 (b). The separated input and output ports allows the co-integration within a more complex PIC.

2. DESIGN AND CHARACTERIZATION OF 4-CHANNEL WBL

Based on the proposed design concept, a 4- channel WBL with a channel spacing 3.2 nm is designed. The basic concept of the proposed WBL design makes use of a 2x8 AWG (schematic shown in Fig. 2(a)) serving as both multiplexing and de-multiplexing structure. The input/output wavelength mapping is such that both the input port

I1 and the output I2 port can be used as both de-multiplexing and multiplexing ports. When I1 is used as de-multiplexer, I2 can be used as the multiplexing port, provided the output ports are connected in pre-designed manner, i.e. the output port O1 is spectrally matched with output port O5, O2 is matched with O6, O3 is matched with O7, and O4 is matched with O8. Fig. 2(b) shows the schematic of the novel WBL design based on a 2x8 AWG with 3.2nm channel spacing, six 90^0-waveguide crossings and four SOA gates. At the input of the WBL, a WDM signal is amplified by a booster SOA, and is de-multiplexed to the output ports O1, O2, O3 and O4. The SOAs at the output are used to pass/block the channels. Channels 1, 2, 3, 4 of the WBL pass through 3 consecutive 90^0 waveguide crossing before being multiplexed at ports 5, 6, 7 and 8 respectively.

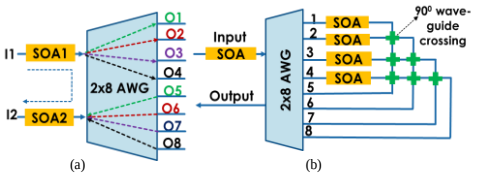

Figure 2. Schematic (a) 2x8 AWG (b) 4-channel WBL based on a 2x8 AWG

To verify the presented design, first the performance of a 2x8 AWG test structure (mask layout shown in Fig. 3 (a)) is characterized. It has two 400 µm SOAs at the two inputs to provide amplification. The spectral profiles measured at the output ports while turning SOA-1 and SOA-2 ON are shown in Fig. 3 (b) and Fig. 3(c) respectively. The measurements are normalized with respect to ASE output of the SOA-1 and SOA-2. The results show the expected spectral matching. Centre wavelengths labelled O1, O2, O3, and O4 in Fig. 3(b) match with centre wavelengths labelled O5, O6, O7, and O8 in Fig. 3(c) respectively which is important for the functionality of the WBL. The cross-talk levels are below -25 dB. Fig. 3 (d) shows the mask layout of the 4-channel WBL based on 2x8 AWG. It has one booster SOA of 900 µm long at the input and 4 SOA gates which are 500 µm long. The spectral profile of the waveguide crossing is individually characterized and is given in Fig. 3(e). It shows the measured fibre-to-fibre loss, when input laser light was swept from 1530-1570 nm. Considering coupling loss variation across wavelengths to vary between 4.8-5.3dB/facet the insertion loss of the crossing is estimated to be 0.3 dB or less. The measured cross-talk level is negligible (< -65 dB).

Next, the spectral profile of the WBL when the booster SOA is injected with 33mA is shown in Fig. 3(f). The measurements are taken at the output port and are normalized with ASE of the booster SOA at 33mA measured at the input port. Hence one can observe the relative gain of the gate SOAs at 60mA compared to the booster ASE output at 33mA. The injection current of the booster SOA and gate SOA for Ch1 are limited to 33mA and 37mA

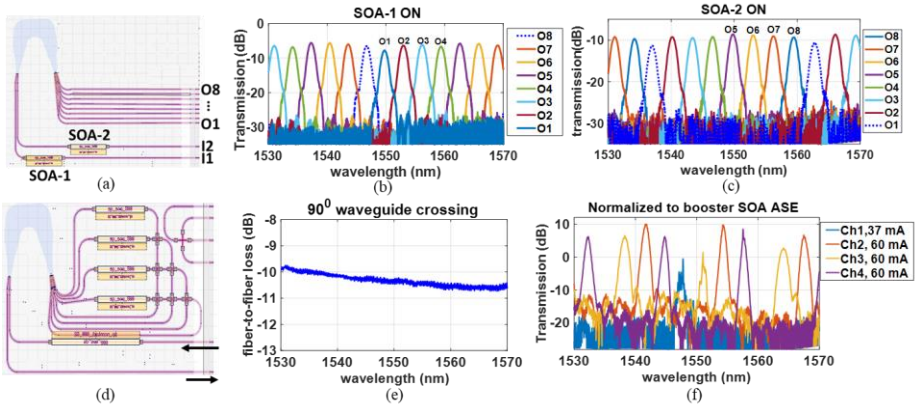

Figure. 3 (a) Mask layout 2x8 AWG (b) spectral profile when SOA-1 is ON (c) spectral profile when SOA-2 is ON (d) mask layout 4-channel WBL (e) fibre-to-fibre loss of 90^0 waveguide crossing (f) spectral profile of 4-channel WBL

respectively because of lasing of these SOAs. This can be improved by improving the quality of AR coatings. All the other gate SOAs are tuned to 60 mA. It can be seen that 4-channel WBL has a channel spacing of 3.2 nm and an FSR of 12.8 nm which is also evident from spectral profile of Ch2, Ch3 and Ch4. Only one peak is shown for Ch1, which is caused by fabrication imperfection affecting the channel periodicity.

3. EXPERIMENTAL SETUP AND RESULTS

Fig. 4(a) shows the experimental setup, where WDM input light sources matching the 4 channels of the WBL are generated by 4 tunable lasers. It also shows the fibre-to-fibre loss measurement of the WBL which is conducted as follows. The polarization state of each input is controlled by polarization controller (PC) before being combined and injected into MZM modulator driven with 10 Gbps, 2^7-1 NRZ data. At the output of the modulator a second PC is used to optimize the polarization state before entering the WBL PIC. The output of the WBL PIC is connected to the optical spectrum analyser (OSA) and EDFAs are not used for the spectrum measurement shown in Fig. 4(a). A single channel is measured at a time by turning the booster SOA and one of the SOA gates. The current applied to the booster SOA is limited at 33mA and gate SOAs are tuned at 60mA except for gate for Ch1 which is tuned

at 37 mA to avoid lasing. The fibre-to-fibre losses (including 5 dB/facet coupling losses) ranged from 7 dB for Ch4 to 22 dB for Ch1. In the future designs, this can be further improved to a very low loss by using a better antireflection coating to avoid lasing so as to drive the booster SOAs at higher current values. The signal-to-neighbouring channels cross-talk level ranges from 26 dB for Ch1 to 33dBs for Ch4. Next, EDFA is introduced before the chip in order to compensate the loss of the MZM modulator. During the measurement, one of the waveguide facets in the WBL PIC was damaged which incurred additional loss of 20 dB at the output of the chip. For this reason a second EDFA is put after the chip to amplify the output power to reach the sensitivity of the PD. Then the BER measurements were taken. Fig. 4(b) and Fig. 4(c) show the BER measurements including the back-to-back measurements for Ch2 and Ch4 of the WBL. The back-to-back measurements were taken after the first EDFA. While doing the measurement, the booster SOAs were tuned only to 23mA and 20 mA for Ch2 and Ch4 respectively to avoid distortion due to lasing. Error-free operation is visible from the BER curves with a power penalties of 1 dB for Ch4 and less than 1.3 dB for Ch2 at BER level of 1E-9. This is also further verified with open

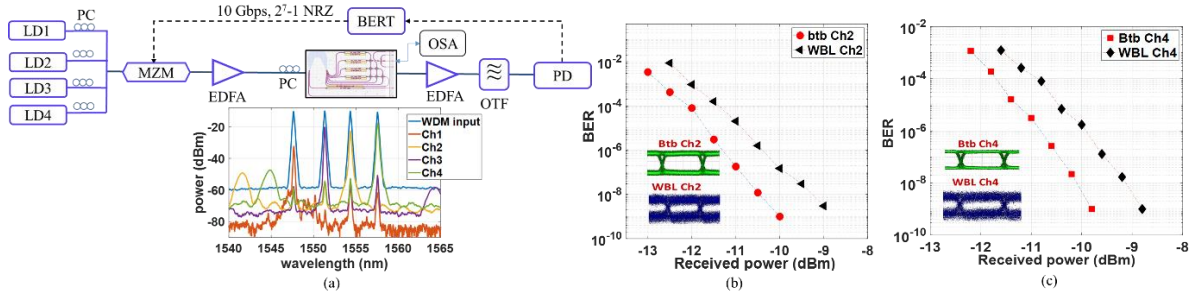

Figure. 4 (a) Experimental setup and spectrum measurement (without using EDFA), measured BER (b) Ch2 (c) Ch4

eye diagrams for both channels. The OSNR level at the input of the chip is 50 dB. At the output of the chip, the OSNR level is 42 dB. The second EDFA is then used to amplify the output power to reach PD sensitivity, hence the worsening the OSNR at the input of the PD to 23dB. The noise distribution on the low and high bit levels as seen in the eye diagram and the power penalty in the BER is therefore caused by second EDFA. In our upcoming work, this presented result will be improved in which we solve the loss at the waveguide facets and avoid lasing of the SOAs to achieve the low-loss performance of the presented WBL design.

4. CONCLUSIONS

We have experimentally verified a novel design of a compact and folded InP WBL based on a single 2x8 AWG and SOA gates. The compact design reduces the number of required AWGs in a WSS by half and supports the scalability of metro core and access nodes. The modularity enables scalability in a pay-as-you-grow fashion. The use of SOAs in the WBL design aids in achieving low-loss performance and low cross-talk level due to high gain and extinction ratio. Hence it proves to have superior performance compared to comparative WBL designs reported in [5, 6]. Transmission of error free 10Gbps NRZ data with <1.3 dB power penalty was recorded.

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