

Discretely tunable optical delay lines using step-chirped subwavelength grating Bragg gratings

(Student's paper)

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ABSTRACT

A discretely tunable optical delay line based on step-chirped subwavelength grating Bragg gratings is proposed and experimentally demonstrated. A total delay of 55 ps in steps of 9 ps is obtained over an operating bandwidth of 29 nm. The device is fabricated using electron beam lithography with a single etch in silicon on insulator.

Keywords: subwavelength grating, silicon photonics, time delay, Bragg grating

1. INTRODUCTION

Integrated optical delay lines are important for signal processing in optical communications and microwave photonics [1]-[4]. One conventional implementation of on-chip optical delay lines uses various lengths of waveguides interconnected by optical switches: the state of the switches is set to obtain different waveguide paths, and hence different delays. In this manner, discrete tuning of the delay can be obtained [1]. Another implementation involves cascading several optical ring resonators; by tuning the phase offset and the power coupling coefficient of the ring resonators, continuous tuning of the delay can be obtained [4]. Finally, continuous or discrete tuning can be obtained using chirped or step-chirped waveguide Bragg gratings (BGs) [5], [6].

Recently, subwavelength grating (SWG) waveguides with low loss and the flexibility in tailoring the effective index have attracted significant attention. Numerous SWG waveguide devices have been realized, including wideband couplers, ring resonator filters, and BG filters [7]. The effective index of the SWG waveguide can be tuned through its duty cycle; thus, SWG waveguides of the same length but different duty cycles will have different propagation delays. We exploited this feature to implement index-variable optical true time delay lines [8]. For SWG waveguides that are 8 mm in length, we observed a differential time delay of ~ 1.6 ps for a difference in duty cycle of 1%.

In this paper, we propose and experimentally demonstrate an integrated discretely tunable optical delay line using SWG waveguide-based step-chirped BGs in silicon-on-insulator (SOI). The step-chirped SWG BG comprises a serial array of ten SWG BGs whose Bragg wavelengths increase linearly with position. We observe a total time delay of up to 54 ps over a 29 nm bandwidth (1524 nm to 1553 nm), with eight discrete delay steps and an increment delay of ~ 9 ps.

2. Device design

The conventional configuration of the SWG waveguide and the simulated effective index are shown in Figs. 1 (a) and (c), respectively; the waveguide cross-section is illustrated in Fig. 1(e). Note that the period and width of the SWG waveguide is 245 nm and 400 nm. All of the effective indices are obtained using 3-D Finite Difference Time Domain (FDTD) simulations [9]. The effective index of the SWG waveguide can be modulated by positioning two loading segments on both sides of the conventional SWG waveguide as shown in Fig. 1 (b) [10]. The simulated effective index of the 'loaded' SWG waveguides for different gap distances as a function of

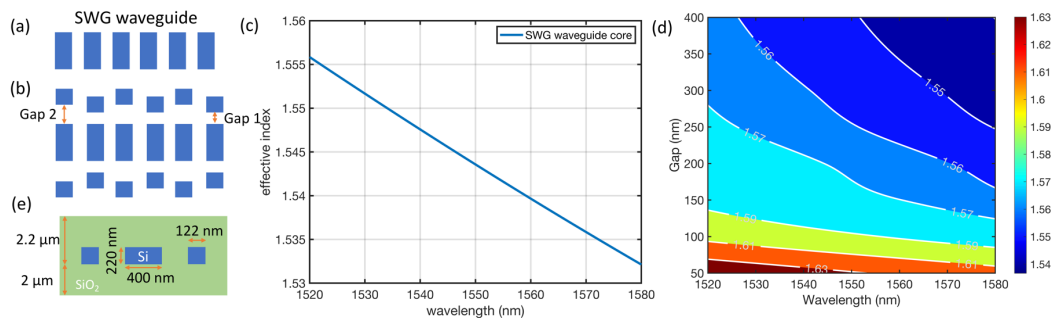


Figure 1. (a) Configuration of the SWG waveguide; (b) configuration of the SWG BGs; (c) simulated effective index of the SWG waveguide in (a); (d) simulated effective index of the 'loaded' SWG waveguides; (e) Cross-sectional view of the SWG BG.

TABLE 1. THE GAPs OF EACH BGs.

(nm)	BG1	BG2	BG3	BG4	BG5	BG6	BG7	BG8	BG9	BG10
Gap 1	381	310	243	217	188	156	139	124	113	104
Gap 2	/	500	356	272	232	207	172	149	133	120

wavelength is shown in Fig. 1 (d). Since the effective index of the ‘loaded’ SWG waveguide can be ‘mapped’ to a gap distance, we can design a SWG BG with specific BG wavelength and bandwidth by picking out the suitable combination of gaps. The designed gaps of each SWG BGs in our step-chirped SWG BG are shown in Table 1. The slash in BG1 represents that no loading segments were used. Theoretically, by directly cascading ten SWG BGs, the designed step-chirped SWG BG can provide ten separate reflection bands with an incremental delay step of ~ 6 ps. The width of the square loading segments is 122 nm and the number of periods in each SWG BG is 1,000. The layout of the device includes two vertical grating couplers (VGCs) for input and output coupling and two tapers for the mode conversion between solid core and SWG waveguides.

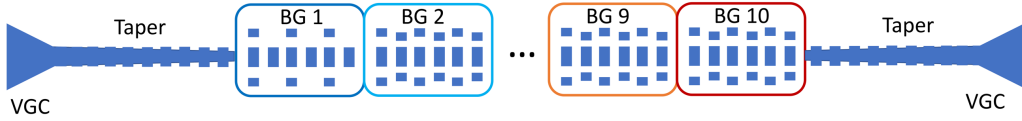


Figure 2. Layout of the step-chirped SWG BG; VGC: vertical grating coupler.

3. Experimental Results and Analysis

Two experiments are conducted to measure the time delay response. First, the group delay is measured directly using an optical vector analyzer (LUNA OVA 5000) as shown in Fig. 3 (a), where a circulator is introduced to measure the reflected signal from the chip. Second, a time-of-flight measurement is used to record the time delay for sinusoidally modulated carriers at different wavelengths, see Fig. 3 (b).

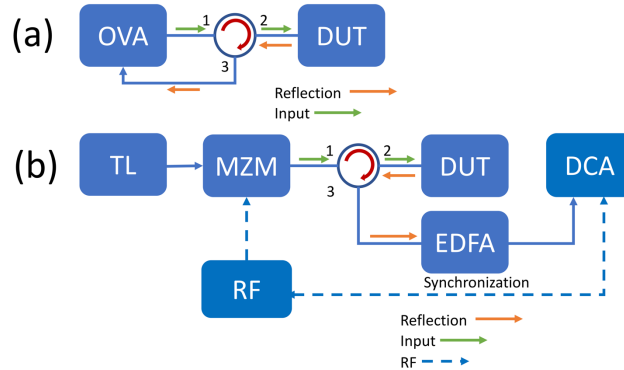


Figure 3. Experimental setup: (a) the measurement of group delay; (b) the time-of-flight measurement; DUT: device under test; EDFA: Erbium-doped optical fiber amplifier; MZM: Mach-Zehnder modulator; TL: tunable laser; DCA: digital communications analyzer. OVA: optical vector analyzer.

Fig. 4 (a) and (b) show the group delays in reflection measured using the OVA. Note that the opposite group delay response is obtained when the input and output ports are reversed. We obtain a total delay of up to 54 ps with an incremental delay of ~ 9 ps. The sinusoidal signals in Fig. 4(c) show clearly an increase in delay with increasing wavelength (we use a signal at 1527 nm as the reference). The time delay steps are given in Table 2.

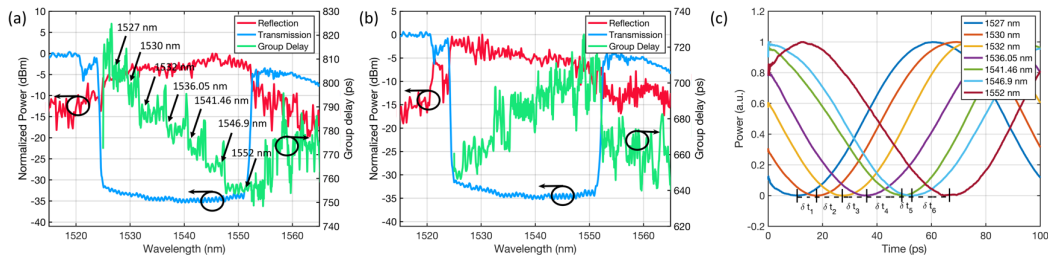


Figure 4. (a) and (b) the measured group delays; (c) the time delay response characterized by DCA.

In contrast to our intended design, we only observe 8 reflection bands. The bands used in the time-of-flight measurements are marked in Fig. 4 (a). According to Table 2, the steps are almost equal at shorter wavelengths; however, the variation is greater at longer wavelengths. The reason is that when we design SWG BGs with a longer BG wavelength, the difference between the two gaps becomes very small (e.g., ~ 20 nm) compared to the fabrication resolution (~ 60 nm). Moreover, a small misalignment of the loading segments will lead to an undesired effective index change, which can cause the shift of the BG wavelength or the expansion of the bandwidth.

TABLE 2. CORRESPONDING TIME DELAY STEPS OF FIG. 4 (C).

Step	δt_1	δt_2	δt_3	δt_4	δt_5	δt_6
(ps)	7	10	8	14	4	11

4. Summary and Discussion

We have designed and experimentally demonstrated an integrated discretely tunable optical delay line in SOI using step-chirped SWG BGs. We realized a total time delay of up to 54 ps over a 29 nm bandwidth; the incremental delay is ~ 9 ps. The device response can be tailored by changing the value of gaps of the loading segments; however, the number of SWG BGs that can be placed in the array is limited in part by fabrication resolution. More specifically, in order to increase the number of steps within a fixed operating bandwidth, more BGs need to be cascaded, and hence a smaller difference between the gaps in a BG is needed. On the other hand, when the number of steps is fixed, adjusting the gap distance of each BG can be used to tune the BG wavelength. A slight modification of the gaps can cause a relatively small shift of BG wavelength. Thus, the fabrication resolution determines the minimum tuning step of the BG wavelength. In order to optimize the performance of the step-chirped SWG BGs, we need to choose suitable gaps between SWG waveguide core and loading segments. Nevertheless, we believe that this provides a new means for tailoring the group delay response of SWG BG structures.

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