GaAs-based gain waveguides with U-bend architecture enabling low loss and high yield hybrid integration on silicon photonic circuits

(Student Paper)

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ABSTRACT

We present a U-bend design for traveling wave III-V gain devices, such as semiconductor optical amplifiers and laser diodes. The design greatly simplifies the butt-coupling between the III-V chip and silicon-on-insulator photonic circuit by bringing the I/O ports on one facet. This removes the need for precise dimension control otherwise required for 2-side coupling, therefore increasing the yield of mounted devices towards 100%. The design, fabrication and characterization of the U-bend device based on Euler bend geometry is presented. The losses for a bend with a minimum bending radius of 83 µm are 1.1 dB. In addition, we present an analysis comparing the yield and coupling losses of the traditionally cleaved devices with the results that the Euler bend approach enable, with the final conclusion that the yield is improved by several times while the losses are decreased by several dB.

Keywords: hybrid integration, III-V, semiconductor optical amplifiers, silicon-on-insulator, coupling losses

1. INTRODUCTION

Silicon photonics and photonic integrated circuits (PICs) provide an attractive platform enabling efficient and flexible signal transfer and processing, which is instrumental for several fields of application, such as telecom, datacom, and sensing. Photonic circuits based on silicon offer low loss waveguides and can be manufactured using existing CMOS facilities. However, their main limitation is the inability to offer optical gain. To overcome this major limitation, heterogeneous, monolithic, and hybrid integration [1] of III-V semiconductors on the silicon platform haves been intensively addressed during the last decade. While heterogeneous and monolithic integration have the advantage of innate alignment of the waveguides between the two material systems, they lack the flexibility of hybrid integration [2], which allows for separate manufacturing of the waveguide platform and the gain chip thus being able to take advantage of the CMOS lines. This is especially advantageous for smaller production volumes and specialized custom devices.

The hybrid integration requires high alignment precision between the Si and III-V waveguides within sub-micron precision. The positioning of the chip can be achieved with the current alignment systems. However, the chip dimension control when using standard methods of scribing and cleaving can result in chip length variation of several microns. Because the pit on the photonics chip reserved for the gain chip is pre-fabricated, the lack of control of the III-V chip dimensions leads to chips too long or short for the designed slot. For devices such as travelling-wave semiconductor optical amplifiers (TW-SOA) with I/O ports at the opposing sides of the chip and with tilted waveguides this can result in significant coupling losses and poor yield.Our solution to this problem is to use a U-bend design for the waveguide of the III-V device where the I/O ports are brought on one side of the chip, as shown in Fig. 1. This design removes the need for precise cleaving and dimension control because only

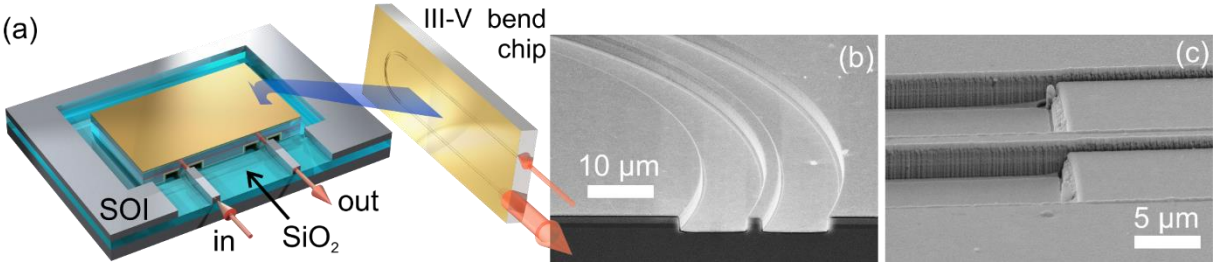

Figure 1. (a) Integration of III-V semiconductor chip with U-bend geometry on silicon-on-insulator (SOI) chip. The I/O ports are on the same side of the chip thus alleviating the requirement for precise dimension control of the chip. (b) Scanning electron microscope (SEM) image of the bend. (c) SEM image of the step between the bent and straight RWG.

one facet needs to be accurately positioned. The U-bend shape is based on Euler spiral design to ensure compact bends with minimized losses [3], [4]. The key features of the design, fabrication and characterization of the U-bend waveguide gain devices and the effect the design has on the yield of the usable devices are discussed.

2. DEVICE DESIGN AND FABRICATION

The Euler bend design has been previously used for Si waveguides to reduce bend losses and has been refined here for use with GaAs-based gain material system. The U-bend consists of two mirror symmetric arcs with a radius of curvature that decreases with increasing arc length with the effective bend radius 1.38 times the minimum bending radius [3]. The minimum bending radius was chosen based on a simulation of the mode propagation through the bend. The simulation used a full-vectorial mode-expansion and tilted overlap integrals resulting in a very efficient three dimensional model [4] and was applied for radii between 1 µm and 200 µm with ridge waveguide (RWG) width varying between 1.0 µm and 2.5 µm. Based on this we chose for testing a 2.5 µm wide ridge with minimum bending radii of 83 µm, 103 µm and 133 µm. The bend area was etched deep through the quantum well structure to ensure lateral mode confinement while the straight sections were etched only until the surface of the topmost cladding layer.

The design was implemented for gain devices operating at 1300 nm wavelength on GaAs with a double quantum well InGaAsN structure, which was placed within 320 nm GaAs waveguide layers itself surrounded by 1 µm $Al_{0.6}Ga_{0.4}As$ cladding layers [5]. The waveguide was defined using two photolithography and dry etch steps, and SiN_x to provide high index difference for improved mode confinement. After this, on the p-side the contact metal layer was deposited followed by a thinning of the wafer to a thickness of 110 µm. Finally, a contact metal layer was deposited on the n-side followed by annealing and cleaving into chips. Although these devices are designed to be used as SOA, for the characterization of the material properties and bend losses the facets of the devices were left uncoated, exhibiting approximately 28% back-reflection to allow laser operation. Typically, our TW-SOA is designed for as small as possible feedback from the facet using proper facet coating and a tilt between WG and facet with approx. 7° angle.

3. CHARACTERIZATION

For the characterization, we used a set of U-bend chips and for a reference a set of RWG chips. The U-bend chips had varying lengths of straight segment of 700 µm, 1700 µm and 3040 µm with varying bend lengths of 519 µm, 645 µm and 843 µm for each straight segment variant. The straight RWG chips had cavity lengths of 800 µm, 1000 µm, 2000 µm and 3000 µm. The devices were operated as laser diodes (LD) at 20°C, in continuous wave mode with bias of 0-200 mA.

The bend loss analysis is based on the derivation of the treatment of Fabry-Perot LDs described by Coldren [6] and is discussed more in depth in [7]. In addition to the standard loss terms: mirror losses α_m and internal losses α_i, we include into the treatment coupling losses α_c from the mode transition from straight RWG into the bend section and the bend losses α_b. As the condition for the device to operate as a LD the losses must equal the threshold modal gain $\Gamma g_{th} = \alpha_i + \alpha_m + \alpha_b + \alpha_c$. By substituting this into the original derivation, we reach an equation

$$\alpha_b = (k_b - k_s)\eta_i ln\left(\frac{1}{R}\right) - \alpha_c \quad (1)$$

where η_i is internal quantum efficiency, R reflectivity and k_b and k_s are the slopes presented in Fig. 2 (a) for bend and straight RWG devices respectively. This derivation assumes the gain equal through the entire bend device. In Fig. 2 (a), the inverse of the differential quantum efficiency η_i is plotted as a function of the cavity length for all measured devices. Here we assume the loss to be the same for all the tested bends as there is no difference between

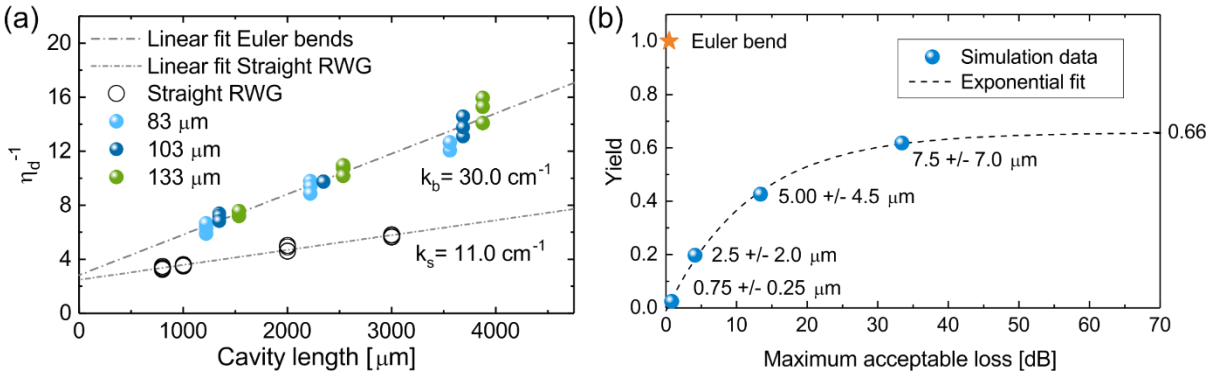

Figure 2. (a) Inverse of the differential quantum efficiency plotted as a function of cavity length for U-bend and straight waveguide devices. (b) The yield of the traditional straight waveguides tilted 7° as a function of the simulated coupling loss.

the slopes between different bends. This assumedly means that the bend radius can still be further decreased without additional losses.

The coupling loss α_c was estimated by using simulation with Eigen Mode Expansion (EME) for the reflectance and transmittance at the step interface. The reflectance was estimated to be 3×10^{-4} and coupling efficiency 89.9% leading to a loss of 0.46 dB. From Fig. 2 (a) we get the values k_b=30.0 cm^{-1} and k_s=11.0 cm^{-1}. With equation (1) we can calculate the total bend loss for the devices to be 9.2 cm^{-1}. For a bend device with 83 µm minimum bending radius and bend length 519 µm the single-pass bend loss is 1.1 dB.

To estimate the impact of the Euler bend design on the integration losses and the yield the coupling loss between 7° tilted SOA chip and 7.257° tilted, 3 µm thick and 4 µm wide SOI waveguides was simulated using Finite-Difference Time-Domain (FDTD) method. As a result, for a coupling with air gap of 0.5 µm reserved for alignment error with the Euler bend chip, the loss was estimated to be 0.3 dB. Simulations were also made for cases with air gaps with certain uncertainties allowed for traditional chips: 0.75 ± 0.25 µm, 2.50 ± 2.00 µm, 5.00 ± 4.50 µm and 7.50 ± 7.00 µm. Resulting maximum losses for each case were respectively: 0.8 dB, 4.1 dB, 13.4 dB and 33.4 dB.

Experiments have shown that the traditional scribe and cleave method provides devices with device length standard deviation of 8.0 µm. We calculated the probability of obtaining devices within the afore mentioned limits by assuming normal distribution and standard deviation of 8.0 µm. These probabilities were then plotted as a function of the calculated maximum losses. The plots presented in Fig. 2 (b) can be fitted with an exponential curve from which we can estimate that maximum achievable yield to be 66%.The yield of the Euler bend devices suitable for integration in regards to their dimensions should essentially reach 100%. This does not take into account any other failure mechanisms, but merely commenting on the need for dimension control of the chips.

4. CONCLUSIONS

We have presented a U-bend design using Euler-bend shape to bring I/O ports of gain waveguides on one facet and reduce coupling losses between III/V gain chips and SOI waveguides when utilizing hybrid integration. The discussion introduced the design, manufacturing and bend loss analysis. Simulation of the coupling losses and an analysis on the improvement in yield when compared to traditional gain chips is discussed.

As an example, we can see that if the maximum acceptable loss is 5 dB, the resulting yield is 22%. In comparison, if we use the Euler bend design, by default the yield approaches 100% with the expected loss of 0.3 dB. Taking into account the penalty of 1.1 dB from the bend losses for 83 µm minimum bending radius the total reduction in losses would be 3.6 dB with a yield 4.5 times larger when using the Euler bend design instead of the traditionally cleaved straight waveguide chips.

ACKNOWLEDGEMENTS

We wish to thank Dr Heikki Virtanen for his help for providing the design for the rib waveguide section. Funding for the RAPIDO project, received under EU FP7-ICT-2013-11, grant agreement no.619806, is gratefully acknowledged.

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