Reduced Timing Jitter in a Hybridly Mode-Locked Semiconductor Laser due to an Increased Modulation Curvature

(Student Paper)

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ABSTRACT

Low-noise microwave oscillators are essential to several applications, and mode-locked lasers are good candidates for the realization of these. The total timing jitter of an actively mode-locked laser has previously been shown to be inversely proportional to the modulation curvature of the driving signal. This paper presents the first numerical study on the timing jitter in a semiconductor hybridly mode-locked laser, when the reverse bias voltage of the saturable absorber is driven with different modulation curvatures. It is confirmed that also for these lasers, the total timing jitter scales reciprocally with the modulation curvature. Thus, according to the numerical model, the performance of a mode-locked laser based oscillator will improve by increasing the bandwidth of the signal driving the saturable absorber. Coupled opto-electronic oscillators, as well as clock extraction from pulse trains in optical time division multiplexing systems, can improve from this.

Keywords: Mode-locked lasers, hybrid mode-locking, timing jitter, photonic integrated circuits, laser modelling, microwave photonics.

1 INTRODUCTION

Generation of low-noise microwave signals is essential for several applications, including Doppler radars [1], and optical communication [2]. Mode-locked lasers (MLL) are promising candidates for such oscillators, especially when incorporated in a coupled opto-electronic oscillator (COEO) [3]. In this, an opto-electronic feedback loop feeds the output of the MLL back to an intra-cavity modular loss element, such as a saturable absorber (SA). Thus, a COEO might be viewed as a hybridly MLL in which the driving signal is a delayed copy of the output from the MLL itself. Thus, it is reasonable to argue that by optimizing the low-noise performance of a hybridly MLL, one also improves the performance of a stand-alone COEO that incorporates this MLL. Also, clock extraction in optical time division multiplexing (OTDM) systems [4] can improve from this.

It has previously been shown, analytically, that the total timing jitter of an actively MLL is reduced when the modulation curvature of the driving signal is increased [5]. For a pure sinusoid this can be done either by increasing the amplitude or the frequency. The analytical expression is short and efficient, but it is based on numerous assumptions, such as small round-trip loss, no saturable absorption, and a Gaussian pulse shape. The aim of this work is to validate the expression for a semiconductor hybridly MLL, in which these assumptions do not hold. The study is based on a numerical model for a semiconductor MLL in which the driving signal is applied to the reverse bias voltage of the SA. In order to keep the validity of the model as high as possible, the parameter values used for the simulation are tailored towards InP based semiconductor lasers, by extracting values from measurements presented throughout literature.

2 METHODS

This work is based on the computationally efficient MLL model developed by Vladimirov and Turaev [6], which consists of three coupled equations. Two differential equations determine the evolution of the saturable gain and absorption, and a third equation governs the evolution of the optical field. The model assumes unidirectional lasing as depicted in Fig. 1(a), which in general is not true for a ring MLL. However, quasi-unidirectional operation can be achieved from an asymmetric cavity configuration [7]. Also, the focus of this study is on hybrid mode-locking (ML), which relates to pulse shaping dynamics and not directly to bidirectional versus unidirectional operation.

A ring MLL configuration with a total cavity length of $4200\ \mu\mathrm{m}$, corresponding to a pulse repetition rate around $20\ \mathrm{GHz}$, is studied. It incorporates a $750\ \mu\mathrm{m}$ long semiconductor optical amplifier (SOA), and a $60\ \mu\mathrm{m}$ long reverse biased SOA, namely a SA. The values for the parameters in this model have been tailored towards the generic InP foundry platform available at SMART Photonics [8], by mostly extracting, either directly or indirectly, values from work related to this platform. Especially important to hybrid ML is the voltage dependency of the SA unsaturated absorption q_0 and carrier lifetime τ_{SA}, presented in Fig. 1(b). Other parameters are listed in the caption of Fig. 1(a). The reverse bias voltage modulation signal is on the form $V_{SA}(t, M) = \Delta V \sum_{m=1}^{M} \frac{1}{M} \cos(m \cdot 2\pi \cdot f_{RF} \cdot t) - V_{bias}$, as depicted in Fig. 1(c). The operating point of the MLL was chosen to $I_{SOA} = 90\ \mathrm{mA}$ and $V_{bias} = 2\ \mathrm{V}$, and passive ML was identified at $f_{PML} = 19.614\ \mathrm{GHz}$.

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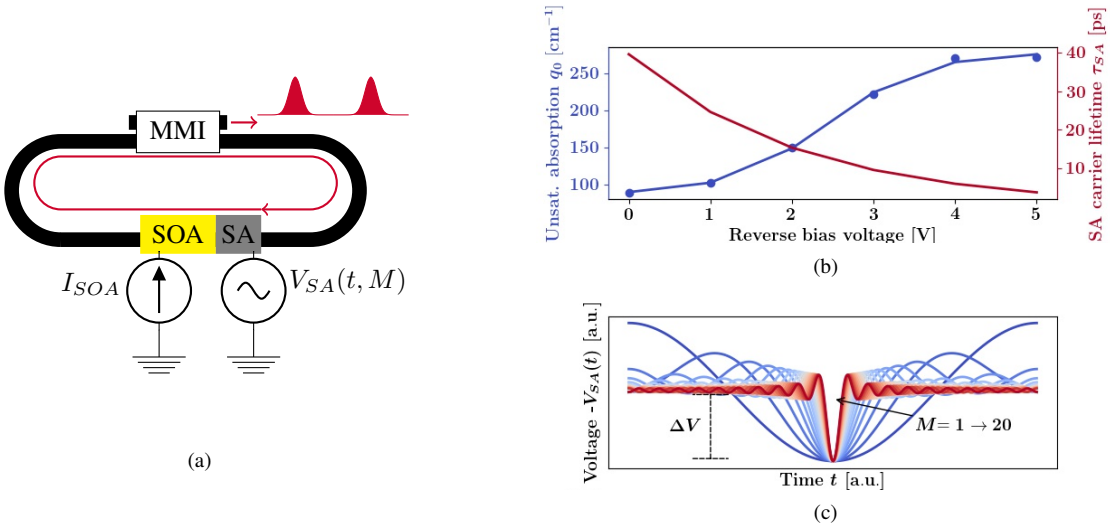
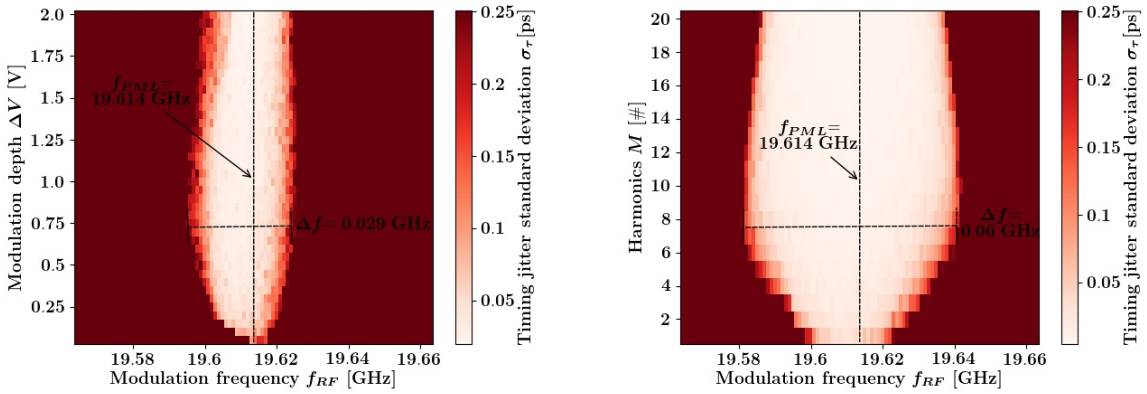


(a) (b) (c)

Figure 1. (a) Schematic of the simulated laser. The following parameter values are used for the simulation: bimolecular recombination coefficient $B = 10^{-16}$ m^3/s [9], SOA transparency carrier density $N_{tr,SOA} = 1.08 \cdot 10^{24}$ m^{-3}, SOA differential gain $a_{N,SOA} = 1.25 \cdot 10^{-20}$ m^2, amplified spontaneous emission (ASE) power spectral density $N_0 = -186$ dBW/Hz, SOA carrier lifetime $\tau_{SOA} = 1.58$ ns, center wavelength $\lambda_0 = 1560$ nm, total gain bandwidth $\omega_L = 12 \cdot 10^{12}$ rad/s [10], stability factor $s = 20$ [11], group velocity $v_g = 8.2429 \cdot 10^7$ m/s, group velocity dispersion (GVD) $k'' = 4 \cdot 10^{-24}$ s^2/m [12], waveguide active area $\sigma_{xy} = 0.0624$ μm^2, confinement factor $\Gamma = 0.074$ [9], SOA linewidth enhancement factor $\alpha_{SOA} = 3$ [13]. The same linewidth enhancement factor is used for the SA $\alpha_{SA} = 3$. The round-trip attenuation factor $\kappa = 0.0884$ is found from the sum of losses due to output coupling in the multi-mode interferometer (MMI), and linear losses in the passive and active waveguides. (b) Plot of SA unsaturated absorption [14] and carrier lifetime [15] vs. reverse bias voltage. (c) Plot of different modulation curvatures of the SA reverse bias voltage.



(a) (b)

Figure 2. Locking range map based on timing jitter standard deviation in a 750 ns interval, for (a) increasing modulation depth and (b) increasing number of harmonics. Values above the free running timing jitter standard deviation 0.25 ps have been rounded to this value.

3 RESULTS

In Fig. 2(a) the locking range is mapped for different modulation depths ΔV when the number of harmonics is fixed to $M = 1$. The locking range is defined as the region for which the timing jitter is below that of the free running MLL. The locking range is asymmetric and the maximum locking range is 0.029 GHz for a modulation depth of 0.75 V. The locking map for an increasing M, and a fixed $\Delta V = 0.5$ V, is shown in Fig. 2(b). The locking range widens for a small M and becomes 0.060 GHz around $M = 7$, after which it narrows.

The phase noise was computed from the output of a 50-μs long simulation, for both free running passive ML, and hybrid ML with $M = 1 \rightarrow 4$. The modulation frequency was fixed to $f_{RF} = 19.610$ GHz, and the modulation depth to $\Delta V = 0.5$ V. The plots are shown in Fig. 3(a), each being an average of 100 simulations. It is seen, from the flattening at lower frequencies, that the random walk is eliminated by locking the MLL to an external ideal clock. Also, it is seen that the flattening level is lowered by increasing the number of harmonics. In accordance with [5] the phase noise is of the form $\mathcal{L}(f) = k_0/(f^2 + f_c^2)$, and fits are shown as dashed black lines. The total phase noise power is found by integrating over all frequencies, leading to the finite value $\pi k_0/f_c$. Taking the root of this and dividing by the oscillation frequency gives the data points for the total timing jitter in Fig. 3(b). According to [5] the total timing jitter variance should be inversely proportional to the modulation curvature, which is given by the second derivative at the minimum of the driving signal, depicted

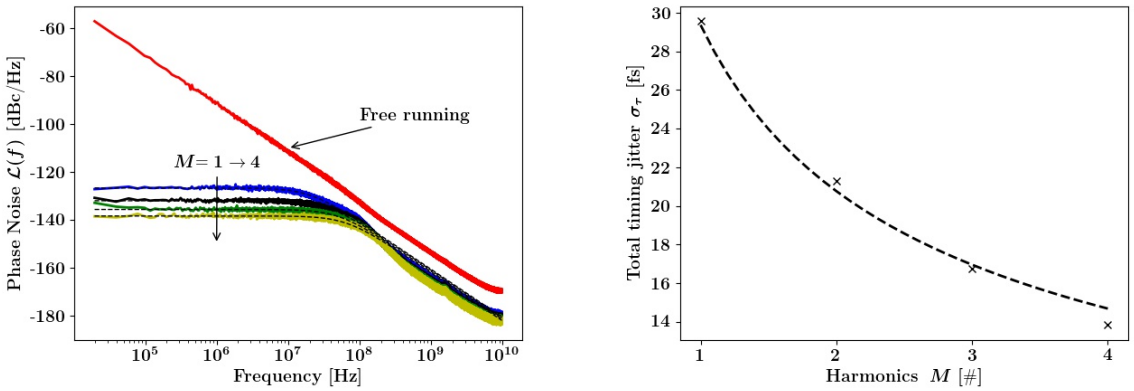


Figure 3. (a) Phase noise of free running and hybridly MLL. (b) Total timing jitter computed from fitted curves in (a).

in Fig. 1(c). Since the signal is assembled from M cosines, the dominating part in the second derivative is the term with the highest frequency, i.e. $(2\pi f_{RF} M)^2 \cdot (\Delta V/M) = (2\pi f_{RF})^2 M \Delta V$. Note that the $1/M$ scaling of the driving signal leads to a linear, and not squared, dependency between the modulation curvature and M. Thus the data points in Fig. 3(b) are fitted to $\sigma_\tau(M) = k_1/\sqrt{M}$, which is shown as a black dashed line.

4 CONCLUSION

It has been shown that the timing jitter of a semiconductor hybridly MLL is reduced just by increasing the number of frequency components, i.e. the bandwidth, of the driving signal. The trend is close to that predicted by the analytical expression in [5]. Thus, this expression is confirmed as a design tool for reduction of timing jitter in a semiconductor hybridly MLL. This result benefits the design of oscillators which incorporate a semiconductor MLL, such as the COEO. The results indicate that the timing stability of this configuration should improve by increasing the bandwidth in the opto-electronic feedback loop. Also, the MLL locks to a wider frequency range when the bandwidth of the driving signal is increased, which makes it more tolerant towards deviations in the oscillation frequency of the external high quality-factor feedback element.

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