Optical transceiver engine based on 12 µm Silicon-on-insulator waveguides and VCSELs

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ABSTRACT

In this paper, we report the fabrication of an optical tranceiver engine that is based on a 12µm silicon on insulator (SOI) waveguide platform and directly modulated vertical cavity surface emitting lasers (VCSELs). The main motivation for using 12 µm thick SOI waveguides is low-loss coupling to standard SM fibers with relaxed alignment tolerances. We demonstrate 25.7Gb/s operation of the complete optical interconnect link channel.

Keywords: silicon photonics, silicon-on-insulator, optical interconnect, VCSEL, hybrid integration

1. INTRODUCTION

In 1–12 µm thick SOI waveguides light is almost completely confined into the waveguide core, so that the effective index is very close to the bulk refractive index of Si (~3.5) and there is very little light at the outer boundary of the Si core. This makes the waveguide components and circuits intrinsically quite insensitive to polarization, dimensional variations and surface roughness. Typical propagation loss in Thick-SOI waveguides is ~0.1 dB/cm. Large waveguide cross-section area also allows to transmit high optical powers (>1 W) without nonlinear absorption. Single-mode (SM) operation over an ultra-wide wavelength range is achieved with rib waveguides [1]. High integration density can be achieved combining SM and adiabatically coupled multi mode (MM) waveguides into the same SM circuit and by using either Euler bends or mirrors [2].

Discrete VCSELs and photodetectors (PDs) already support 28 Gb/s on-off keying (OOK), which shows a path towards 50-100 Gb/s bandwidth per wavelength by using more advanced modulation formats like PAM4. Directly modulated VCSELs enable very power-efficient optical interconnects for up to 40 km distance. There are inherent advantages in combining directly modulated, long wavelength, single mode VCSELs with thick SOI waveguides for transceiver applications. Due to direct VCSEL modulation there will be no need for high speed waveguide modulator which simplifies significantly the Si photonics chip design and fabrication. In addition, there is no need for spot-size conversion between the SOI waveguide and fiber as their mode fields match well with each other. Also, high speed PDs with sufficiently large optical aperture are available.

2. SOI WAVEGUIDE FABRICATION

The 12 µm SOI chip design is shown in Fig. 1 (left). At the bottom of the layout there is one set of four waveguides connecting to four VCSELs, and another connecting to four PDs. These waveguides are routed to another edge of the 12 µm chip for coupling into a single SM fiber array. Chip contains also an alignment loop from one SM fiber to another, which can be used in the alignment of the I/O fiber array.

In the fiber I/O interface we use 12.5 µm wide rib type SM waveguide that is followed by a rib-strip converter and 12 µm thick and 12 µm wide strip waveguides. For the VCSEL coupling, the waveguide thickness and width is reduced to 8 µm in order to better match the SOI waveguide and VCSEL mode fields. In the PD coupling, the waveguide thickness and width are both 12 µm.

SOI chip size is only 4 mm by 5 mm. We are using 90° total internal reflection (TIR) mirrors for waveguide turns. Transmitter and receiver waveguides have all also one waveguide crossing on their path. These crossings are low loss in wide waveguides as used here. The fabricated chip is shown in Fig. 1 (middle). Fabricated waveguides have good quality etched side-walls and TIR mirror facets (Fig. 1 (right)). Chip facets have been polished after dicing and an antireflection coating (ARC) has been deposited on chip level using atomic layer deposition (ALD). We have used 143 nm thick TiO_2/Al_2O_3 nanolaminate as an ARC.

3. VCSELs

Vertical Cavity Surface Emitting Lasers (VCSEL) are attractive for the optical interconnects thanks to low power dissipation and suitability for dense integration. Long-wavelength VCSELs operating at 1.3 and 1.55 µm are compatible with Si waveguides. The lasers employed in this paper consist of single-mode short-cavity 1.3µm VCSELs manufactured by Vertilas [3]. The VCSEL structure is based on Vertilas' InP Buried Tunnel Junction design and features a very short optical cavity. VCSELs exhibit a 3 dB-modulation bandwidth of up to 17 GHz (at temperature of 20°C). [1]

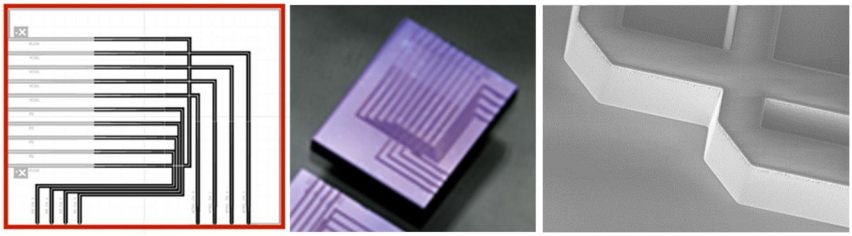

Figure 1.Left: SOI chip design with I/O ports for transmitter and receiver fibers and active alignment fibers, VCSELs and PDs. Middle: 4x5 mm chip with 12µm waveguides for routing of signals between fibers, VCSELs and PDs. Right: A scanning electron microscope image of TIR mirrors and crossings in 12 µm SOI.

4. HYBRID INTEGRATION

We have studied several integration concepts for the transceiver implementations based on hybrid integration of 12 µm SOI waveguides, VCSELs, PDs and standard SM fibers. Recently a demonstrator transceiver assembly with 4+4 channels was designed and built, including also transceiver electronics for 25 Gb/s/channel operation. The integration concept of the transceiver demo is illustrated in Fig. 2. Essentially, all the (opto)electronics was built on a printed circuit board (PCB) and then the fiber-pigtailed 12 µm SOI chip was vertically assembled on top of the PCB. This way the VCSELs and PD array were edge-coupled to the SOI waveguides at the chip facet.

The assembly process was as follows: Four discrete VCSEL dies from Vertilas were first bonded on a Si submount with ~1 µm alignment accuracy. Then this subassembly and a 4-channel PD array (4x28 Gb/s by Albis Optoelectronics) were bonded on the PCB with high precision. In addition, four-channel VCSEL driver and receiver ICs (by MACOM) were bonded right next to the VCSELs and PDs, so that very short wire-bonds could be made between them. This enabled good signal integrity for the targeted 25 Gb/s operation. Separately, the 12 µm SOI chip was aligned and adhesive bonded to a fiber-array v-groove assembly. This modular assembly approach allowed testing of the optoelectronic parts before adding the fiber-pigtailed SOI chip on top of the optoelectronic subassembly. Moreover, it allowed powering the VCSELs and the receivers while aligning the pigtailed SOI chip to them, thus enabling active alignment. All 4 VCSEL and 4 PD channels could be simultaneously aligned to their corresponding waveguide facets, thanks to the accurate positions of those active devices on the PCB. After the active alignment, the SOI chip and fiber array subassembly was fixed to its position by adhesive bonding.

The complete assembled transceiver demonstrator is shown in Fig. 3. The PCB also includes 16 pieces of high-frequency coaxial connectors for the differential electrical input and output channels of the optical transceiver.

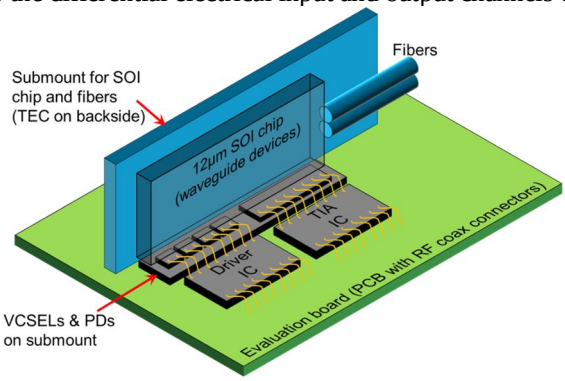

Figure 2. The integration concept of the transceiver demo. All the (opto)electronics is built on a PCB before the vertical assembly of the fiber-pigtailed 12 µm SOI chip.

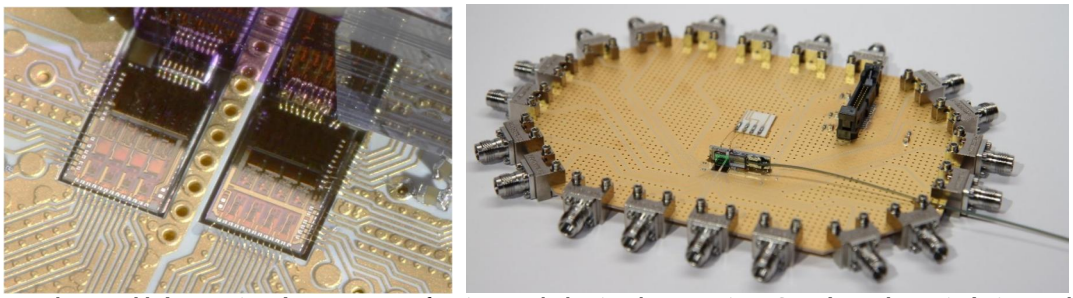

Figure 3. The assembled transceiver demonstrator. Left: Micrograph showing the transceiver ICs and optoelectronic devices on the PCB as well as the part of the SOI chip and fiber array on top of them. Right: Complete demonstrator.

5. CHARACTERIZATION

5.1 SOI chip

The channel losses for all VCSEL and PD channels were measured on chip level before the assembly. The waveguide losses were measured with SM fibers at both ends of the waveguide and with index matching oil in the fiber-chip interface. Measured losses were 1-2dB in the PD channels and 3-5dB in the VCSEL channels. In the VCSEL channels the loss is increased mainly because of the mode field mismatch between the 8µm by 8µm and SM fiber. In addition, some minor loss is expected also from waveguide tapering in the VCSEL waveguide.

Losses in the TIR mirrors are low. The loss measurement of TIR mirror test structures that were processed in the same process run, showed approximately 0.15 dB/90° loss over a wide wavelength range [2].

5.2 Optical coupling

The demonstrator assembly enabled characterisation of the various coupling losses and alignment tolerances. During the assembly process, the alignment sensitivity of the VCSEL and the SOI waveguide coupling was analysed. Approximately 1 µm transversal alignment requirements were measured for the 1 dB excess loss tolerance of the VCSEL-to-waveguide coupling [2].

The fiber-to-SOI waveguide coupling loss was measured by applying a waveguide loop circuit on the chip, which enabled routing the optical power back to another fiber channel of the fiber array (and thus active alignment during the fiber pigtailing process). This loss that includes both the fiber-to-SOI and SOI-to-fiber interfaces and the waveguide chip losses was 3-4 dB in total after the adhesive curing.

The total fiber coupling losses from the VCSELs (through the SOI waveguides) were measured ca 7-8 dB. Correspondingly, the total insertion losses from the fibers to the PDs (through the SOI waveguides) were measured ca 2-3 dB. Consequently, the overall loss of the optical data link was approximately 10 dB in the demonstrator.

5.3 Data link

The performance of the optical interconnect was characterised too. A complete optical data link was established by connecting the output fibers of transmitter channels to the input fibers of the receivers. An eye-diagram of the complete link channel operating at 25.7 Gb/s is presented in Fig 4.

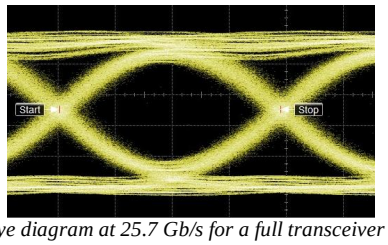

Figure 4. Measured eye diagram at 25.7 Gb/s for a full transceiver link (with CDR).

6. CONCLUSIONS

We have reported the fabrication of an optical transceiver engine that is based on a 12µm SOI waveguide platform and directly modulated VCSELs. A 25.7Gb/s operation was demonstrated for the full link channel. This transceiver concept is a simple and low cost compared to transceivers fabricated on the mainstream sub-micron SOI or even 3µm SOI platform, as there is no need for on-chip modulator or mode size converters between the waveguide chip and optical fiber. The 12µm SOI platform also enables the realization of Nx1 wavelength multiplexers/demultiplexers based on asymmetric Mach-Zehnder interferometers (AMZIs) or echelle gratings.

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