First Silicon Photonics Coherent Receiver With Heterogeneously Integrated III-V On Silicon Tunable Local Oscillator Operating At 28 GBd Data Rates

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ABSTRACT

We demonstrated the first coherent receiver with III-V on silicon monolithic integrated local oscillator. It shows clean QPSK constellation at 28 GBd with $1.7\,10^{-4}$ BER, and a footprint shrunk to 2 mm x 1.5 mm. The local oscillator presents a 45 nm tuning range obtained by thermally tuned Vernier filter. The compactness of the rings ensures a reduced power consumption of 200 mW sufficient to span the whole tuning range. The local oscillator shows a narrow linewidth of 150 kHz compatible with high speed coherent detection.

Keywords: Silicon Photonics, Coherent Detection, III-V on Silicon Monolithic Integration, Photonic Integrated Circuits

1 INTRODUCTION

The world data traffic is increasing exponentially since 1995, it is expected to be 100 $ZB/Month$ in 2020 [1]. Coherent transmission is a key technology to handle this huge data traffic. It enables advanced formats using both phase and amplitude modulations which ensure high spectral efficiency at high bit-rate per optical channel. To support a typical 400 Gb/s data-rate per fiber at affordable costs, silicon photonics is a very good candidate with its high integration level and low cost [2]. This platform is particularly suited for coherent receivers which require a large number of passive and active functions.
We report the first fully integrated coherent receiver (CR) achieved by monolithic integration of III-V on silicon local oscillator (LO). The silicon on insulator wafers (SOI) were fabricated using 200 mm pilot line CMOS processing tools (LETI), including the molecular bonding of III-V, while the III-V process and metallization was performed in a conventional III-V fab [3]. Integration of LO is a major advance for silicon coherent receiver. The integrated LO shows a very narrow linewidth of 150 kHz, and an output power in the Silicon waveguide around 5 dBm. That alleviates the usual coupling losses encountered with external LO. Furthermore BER measurements show no evidence of penalty related to the III-V on Silicon integration process.

2 PRELIMINARY CHARACTERIZATIONS

The schematic and layout of the chip are shown in Fig. 1 a) and b). The integrated local oscillator is a III-V on SOI tunable laser based on double-rings Vernier effect [5], with a InGaAlAs multi-quantum wells gain structure. The external input signal is coupled with a grating coupler and coherently mixed with the LO using a MMI (Multi-Mode Interferometer) 90° hybrid. 4 photodiodes (PDs) provide the beating notes enabling the quadrature demodulation principle. The PDs and LO share the same III-V epitaxy.

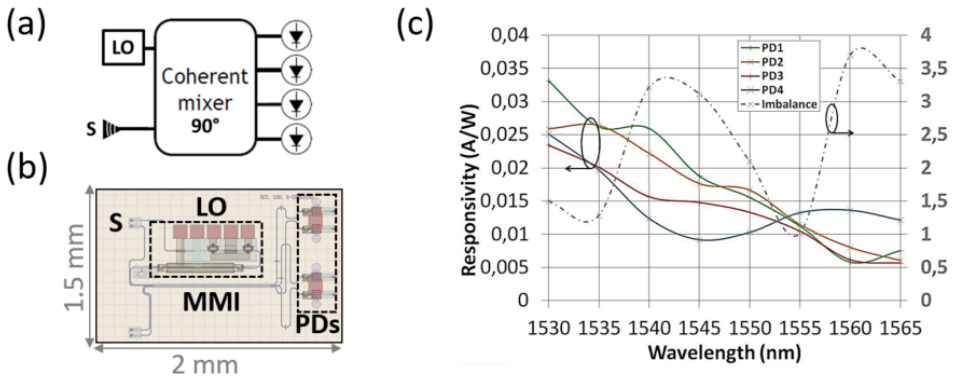

Figure 1. a) Generic schematic of coherent receiver b) Layout of the chip. c) On-chip PDs measured responsivity using external signal output while the local oscillator is turned off.

As shown in Fig. 1 c) the net responsivity of the on-chip PDs is around $0.025\,A/W$ at 1530 nm with an imbalance of 1 to 3.5 dB. The net responsivity includes fiber-to-chip coupling losses and MMI losses. MMI characterizations show a shifted transmission maximum to shorter wavelengths around 1520 nm as shown in Fig. 2 a). The MMI length must vary with the square of its width, for this CR, we had chosen a short MMI design of 1 mm which is more sensitive to manufacturing hazards [4]. That plausibly explains the shift of the MMI maximum transmission. Fig. 2 b) shows a stand-alone PD responsivity reverse biased at -1 V (maximum absorption bias). PDs are more responsive at high wavelengths in the C-band, this behavior is repeatable for all the reverse biased PDs throughout the 3 inches wafer. The PDs maximum responsivity is around $0.6\,A/W$, which is comparable to Ge-on-Si PDs [7]. Furthermore vertical coupler and gain structure are also centered at 1550 nm. Because of mismatch between MMI, gain, and PD maximum responses, we are a couple of dB below the optimal performances of the device.

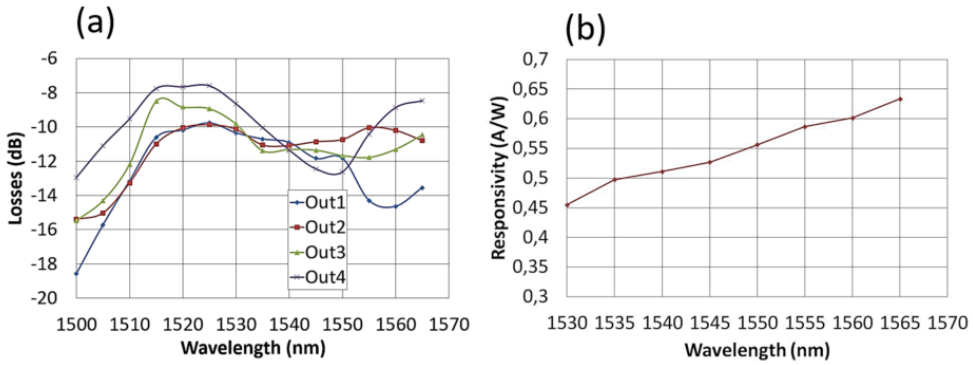

Figure 2. a) Transmission losses of the MMI. b) Stand-alone PD measured responsivity as a function of wavelength.

3 STAND-ALONE LOCAL OSCILLATOR CHARACTERIZATIONS

The laser used and shown in Fig. 3 a) comprises two Sagnac mirrors (M1 & M2), two ring resonators for the Vernier effect (R1 & R2), a phase control section, and III-V gain medium. To achieve the mode transition between the SOI and the InP bonded chip, we use tapers on the silicon waveguide which ensure a mode-index matching region between the III-V and the silicon waveguides. For the stand-alone test device, fiber grating couplers (FGC) are used to extract the light into vertical fibers. We obtain a 45 nm tuning range (see Fig. 3 c)), a 30 mA threshold current, and an fiber coupled power of 1 mW. We also performed a measurement of the power spectral density (PSD) of the LO frequency noise according to the self-heterodyne method, we obtain a 150 kHz Schawlow-Townes linewidth at 1 mW on-fiber output power, see Fig. 3 b).

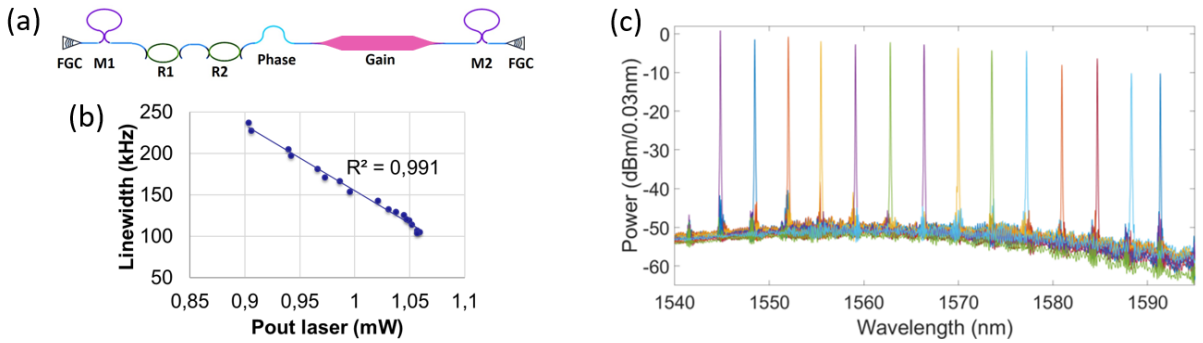

Figure 3. a) Design of the integrated tunable III-V on silicon LO. b) Laser linewidth measurement as a function of the output power. c) 45 nm measured tuning range

4 ON-CHIP CONSTELLATION MEASUREMENTS

The full chip was tested with the setup of Fig. 4 c). A tunable external laser source provides the signal. The later is modulated by an IQ-modulator (30 GHz Lithium Niobate MZ modulator) driven by a DAC and split by 50/50 coupler. One part is sent to an OSA to monitor the modulation shape, notably controlling the carrier-suppression, the other part is sent to the chip with a single mode fiber (SMF) after EDFA amplification.

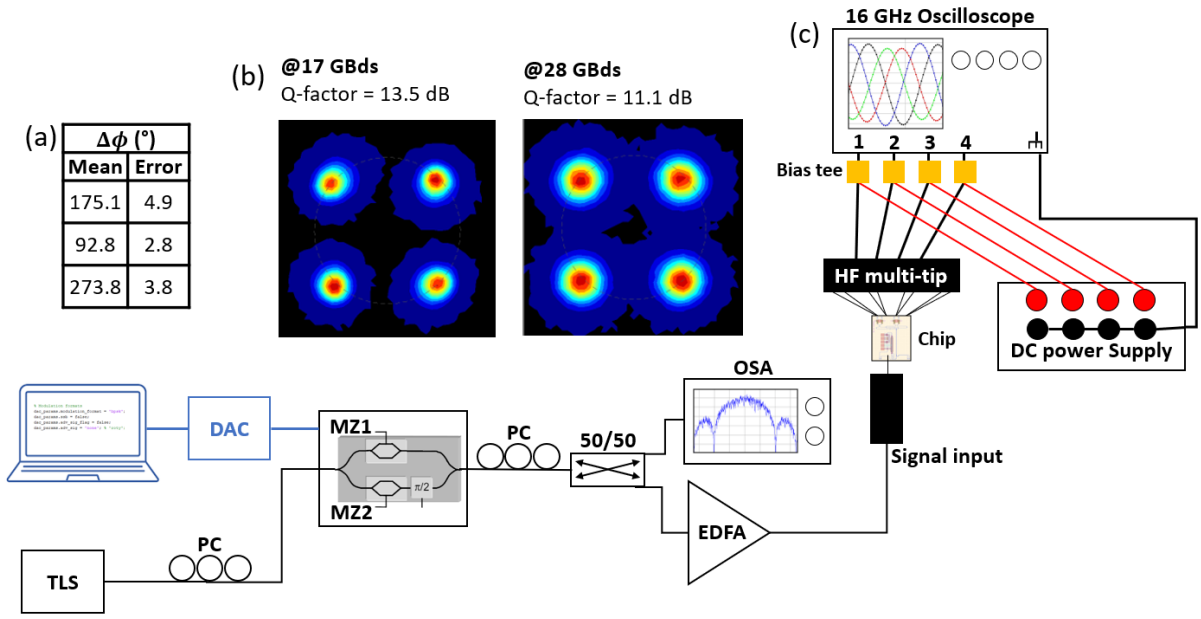

Figure 4. a) Measured dephasing errors. b) Measured constellations at 17 GBd & 28 GBd. c) Schematic of the experimental setup

The beating between the signal and the local oscillator is measured to extract the phase response. We obtain less than 5 degrees phase error for the quadrature demodulation dephasing at $180°$, $90°$, and $270°$ as shown in the table, Fig. 4 a). These results are within current system specifications for coherent receivers, and show no evidence of any impact of LO integration on SOI CR platform. To measure the constellation, the desired PRBS is generated by a Matlab script and sent to a DAC that drives the IQ-modulator in QPSK mode. After a DSP stage we obtain clean on-chip constellations, with $1.1\,10^{-6}$ BER at 17 GBd and $1.7\,10^{-4}$ BER at 28 GBd (Fig. 4 c)), it's comparable with the BER obtained in silicon photonics CR with external LO. These measurements were performed at 1545 nm wavelength, it was the shortest wavelength achievable by the integrated LO. That limits the optical received power by PDs as explained in the first paragraph. Performances are also partly limited by the experimental setup: low voltage on the oscilloscope due to on-chip experiments without TIA, and low oscilloscope bandwidth at 16 GHz.

5 CONCLUSION

We performed the first fully integrated III-V on silicon coherent receiver with LO, fabricated on 200 mm pilot line CMOS processing tools. It shows a 28 GBd QPSK constellations whose intrinsic BER does not exceed 10^{-4}. This important result shows the potential of silicon photonics for process industrialization, high level integration in compact PIC, and high speed operation. CMOS compatible process of III-V on silicon devices might be an appealing way to co-integrate the high performance Germanium photodiodes with the hybrid III-V on silicon LO for the next generation of coherent receiver [8]. This will enable to face the challenges of transmitting huge volume of data in long-haul and metro applications at low costs.

REFERENCES

[1] M. K. Weldon, *The Future X Network: A Bell Labs Perspective*. CRC Press, 2016.

[2] R. Soref, "The Past, Present, and Future of Silicon Photonics," IEEE J. Sel. Topics Quantum Electron., vol. **12**, no. 6, p. 1678-1687 (2006).

[3] G. Duan et al., "Hybrid III–V on Silicon Lasers for Photonic Integrated Circuits on Silicon," IEEE J. Sel. Topics Quantum Electron., vol. **20**, no. 4, p. 158-170, (2014).

[4] X. Pommarede,"Circuits photoniques intégrés III-V/Si pour les applications en télécommunications optiques," Ph.D. dissertation, Univ. Paris Saclay, Accessed on: April, 2017, Available: http://www.theses.fr/2017SACLC020/document

[5] H. Elfaiki et al., "Ultra Wide Hybrid III-V On Silicon Tunable Laser," Proc. ECOC, We3C1, Roma, Italy, Sept 23–27. 2018.

[6] C. Baudot et al., "Developments in 300mm silicon photonics using traditional CMOS fabrication methods and materials," IEEE International Electron Devices Meeting (IEDM) 34.3.1-34.3.4 (2017).

[7] L. Virot et al.,"High-performance waveguide-integrated germanium PIN photodiodes for optical communication applications [Invited]," Photon. Res. **1**, 140-147 (2013).

[8] B. Szelag et al., "Hybrid III-V/Si DFB laser integration on a 220 mm fully CMOS-compatible silicon photonics platform," IEEE International Electron Devices Meeting (IEDM), 24.1.1-24.1.4 (2017).