Monolithically Integrated Wavelength-Selective Switch on InP: a Circuit Simulation-Based Design Study

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ABSTRACT

Flexible optical networks have pushed the need for fast and compact switching elements. A wavelength-selective switch consisting of passive arrayed waveguide gratings (AWG)-based multiplexers and demultiplexers and active semiconductor optical amplifier (SOA)-based optical switches is presented and analyzed in detail by means of hybrid time-and-frequency-domain simulations. The performance of the component is investigated and discussed.

Keywords: Wavelength Selective Switch, AWG, SOA, Elastic Networks, Simulations, Photonics.

1. INTRODUCTION:

Next generation metro and inter-datacenter networks are required to achieve highly-efficient bandwidth utilization, enabled by the use of programmable and elastic physical optical network. Flexible and sliceable transponders, controlled by software-defined networking, promise to greatly optimize hardware resource utilization and lower costs and thus constitute the key technology for future networks [1]. All this places new and strict requirements on reconfigurable optical add/drop multiplexers (ROADMs) of which wavelength selective switches (WSS) are a the main building block. Monolithically integrated solutions are particularly attractive as they allow for faster switching, less area, and fewer optical interfaces. Recently, integrated WSS have been demonstrated for large channel spacing (500 GHz) and 4 wavelengths [2,3]. However, in practical systems employing dense wavelength division multiplexing, a WSS with larger number of channels and narrower channel is required. Scaling the number of channels with narrow channel spacing demands accurate design and performance analyses and should take into account the technology platform adopted to fabricate the circuit.

A very-high-speed 1×4 integrated WSS enabling control of 64 12.5-GHz wide frequency slices is the topic of this paper. The WSS operates over 800 GHz in the C-band and is based on the assembly of four 64-λ monolithic wavelength blockers (WBLs). The 64-λ WBL prototype here presented targets a switching time < 20 ns and is designed to be compatible with the Flex-Grid ITU standard. The proposed architecture includes Mach-Zehnder Interferometer (MZI) interleavers, arrayed waveguide gratings, and a set of active semiconductor optical amplifiers and is to be fabricated as a photonic integrated circuit (PIC) in the generic InP platform by SMART Photonics.

2. WAVELENGTH-SELECTIVE SWITCH

The fast InP 1×4 WSS will follow a broadcast-and-select architecture that allows individual control of each 12.5-GHz spectral slice to each of its outputs (Figure 1). The basic principle of operation of the 1×4 WSS involves two stages in a similar fashion as the work reported in [2,3]: in stage-1 the input signal is broadcasted via a 1×4 splitter; in stage-2 four identical WBLs, based on AWG DeMUX/MUX units and SOA switches, are used (Figure 1-a). Within a DeMUX/MUX element, a first set of AWGs is used to de-multiplex the different wavelengths. Current-driven SOAs are used to turn on and off each individual wavelength at the desired output. Finally, an additional set of AWGs and power combiners (PCs) are used to multiplex and combine the several wavelength slices, potentially amplified or filtered, back into a single channel routed to the PIC's output. The switching control is performed via externally applied electrical signals. Employing SOAs as switches has the advantage to provide on-chip amplification that compensates the losses introduced by the two AWGs, routing, and coupling: by tuning the electrical drive, the optical power of each output slice can be precisely adjusted. It also enables the independent control of each spectral slice (channel) with a switching time less than 20 ns.

The straight forward implementation of the 1x4 WSS calls for AWGs with 12.5 GHz channel spacing, which occupies a large wafer space and are practically prohibitive. To counteract this and significantly reduce the device footprint, an interleaver is employed together with AWGs with larger channel spacing: an interleaver with N output ports makes it possible to reach the target specifications by incrementing the number of DeMUX-MUX units to $4 \cdot N$ while decreasing the number of processed wavelengths per WBL to $64/N$ and increasing the required AWG channel spacing to $12.5 \cdot N$ GHz. In the proposed design, a 1:8 interleaver is used to de-interleave the dense 12.5 GHz into a sparser 100 GHz spectral grid. The total number of DeMUX-MUX elements increases to 32,

whereas the number of wavelengths within each elements decreases to 8. Finally, AWGs with a channel spacing of 100 GHz, expected to lead to a much larger yield, are used. Each of the DeMUX-MUX units within one WBL prototype is designed with a center frequency shifted of 12.5 GHz with respect to the previous one.

The 1:8 interleaver outputs' FSR are to match the channel spacing of the WBL, namely 100 GHz. The proposed design achieves this by implementing a three-stage cascaded imbalanced MZIs architecture (Figure 1-b). The first, second, and third stage are designed to have a channel spacing of 12.5 GHz, 25 GHz, and 50 GHz, respectively. In order to develop a flat top characteristic response, the first and second stages of the interleaver make use of 3 and 2 MZI units, respectively. Fine control of the power coupling ratio and the phase values are essential to maintain the functionality of the interleaver and can be obtained via the implementation of externally controlled phase shifters [4], not included in the prototype.

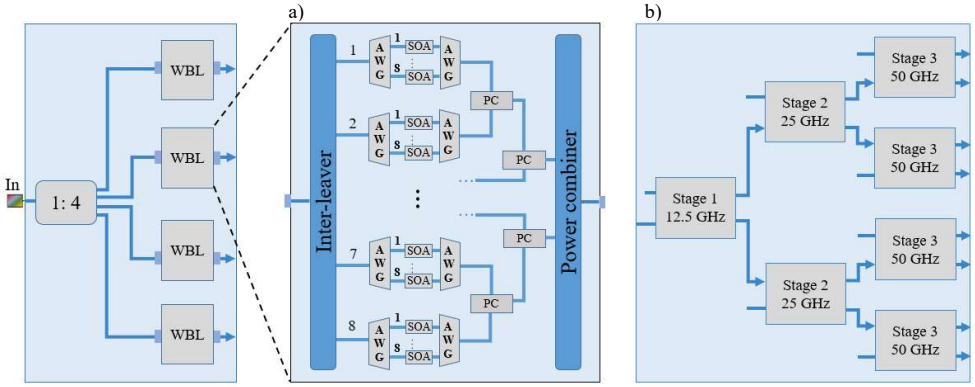

Figure 1: Architecture of the 1×4 fast WSS and detail of (a) one of the four 64-λ WBL prototypes and (b) the 1:8 interleaver

3. SIMULATION SETUP AND RESULTS

The 64-λ WBL prototype includes 11 MZIs within the interleaver and 16 AWGs plus 64 SOAs for the DeMUX-MUX stages. The large number of monolithically integrated components makes it hard to perform fast and reliable evaluation via simulation of the complete WSS. In addition, the coexistence of several passive and active photonic elements, namely the AWGs and the SOAs, poses a further challenge. Whereas the former are best described in terms of their time-invariant frequency response, the latter require the simulation to be performed sample-by-sample in time domain to properly account for their non-linear dynamics. The modeling of passive components in time domain is performed by constructing digital finite-impulse-response (FIR) filter equivalents. This constitutes a critical task: the unavoidable limited accuracy of each FIR representation quickly worsen their impact due to multiplicative effects and the large number of components in the design [5]. To overcome this issue and accurately model the device, the WBL prototype is investigated using VPIcomponentMaker Photonic Circuits using the hybrid time-and-frequency-domain approach [6].

The simulation model carefully mirrors the design architecture. Because of the large number of repeated identical sub-units, i.e. the several SOAs on a deeper level and the DeMUX/MUXes above, a hierarchical setup allows for the model to be built with just few building blocks. The DeMUX/MUX cell has a single input and output and contains a 1x8 AWG, 8 SOAs with associated quasi-DC drive, and a 8x1 AWG (Figure 2). The two AWGs are identical, but mirrored, and are assumed lossless for the early investigations. The SOAs are modeled with a sophisticated optical traveling-wave approach and include carrier dynamics and noise. The gain curves of the SMART Photonics InP SOA component are implemented: at 1550 nm net gain equal to 60 cm^{-1} is achieved for a pump current density equal to 9 kA/cm^2, whereas absorption of 230 cm^{-1} is obtained when no current is driven [7].

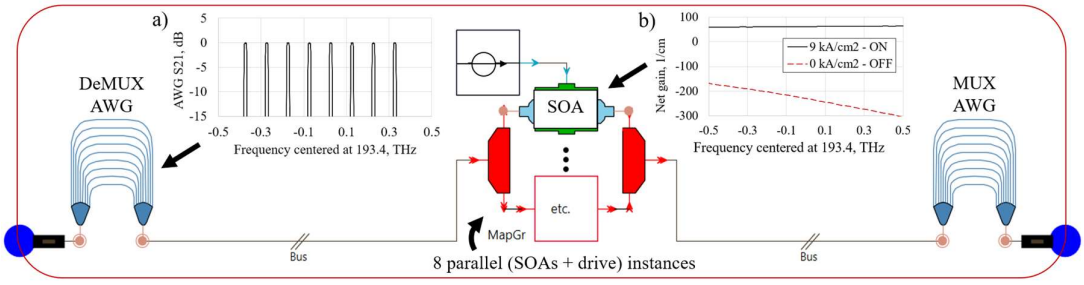

Figure 2: MUX-DEMUX unit setup including a current-driven SOA per AWG channel with detail of (a) the AWG transfer function and (b) the gain of the SOAs in the 'on' and 'off' state.

The WBL unit is simulated by instancing 8 parallel DeMUX-MUX cells, by routing each of the interleaver outputs to a different cell, and by recombining their output power into a single channel (Figure 3). The SOAs are 1.5 mm long and are driven with a pump current density of 9 kA/cm^2 for the 'on'-channels and with no current for the 'off'-channels. The steady-state frequency response of the WBL prototype is simulated for different drive configurations showing the switching capability of the unit (Figure 4). The slightly slanted transfer function is to be attributed to the SOA gain, which is increasing for higher frequencies, and can be adjusted by simply fine tuning the several pump currents. Additionally, notches are observed in the recombined output spectrum between the different slices. These are due to small misalignments between the interleaver's and DeMUX-MUX's slices and can be avoided by increasing the bandwidth of one of the two components.

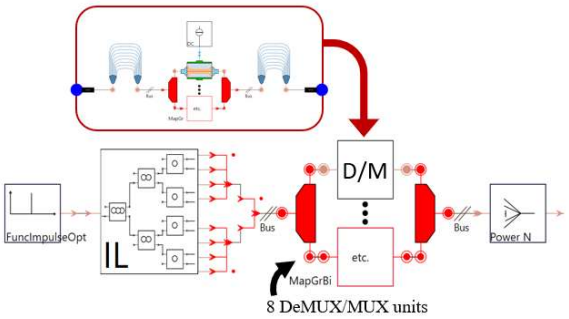

Figure 3: 64-λ WBL simulation setup including a 1:8 interleaver (IL) and 8 parallel DeMUX/MUX (D/M) units

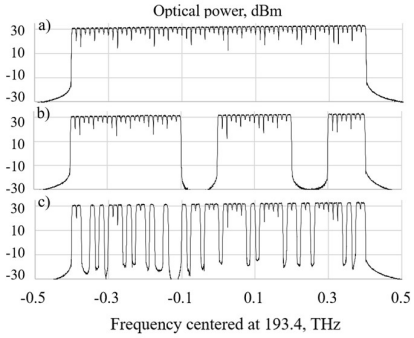

Figure 4: Steady-state transfer characteristic of the WBL (a) at max gain, (b) with 4th and 7th SOA-channels switched off, and (c) with arbitrary slicing drive.

As further test, a raised-cosine binary signal with 0.05 roll-off is fed to the interleaver input by replacing the impulse source with an optical transmitter. In order to test the WSS dynamic operation, a 10 GBd signal fitting into a single 12.5 GHz slice is launched into the structure. The immediately adjacent channels are switched on and off to investigate their impact, while all other channels are kept off. The active channels are driven with 1.5 kA/cm^2 pump current density. It is observed how the output signal spectrum is affected in the two cases and that the signal suffers only from little distortion passing through the WBL. As expected, due to the fact that the launched signal is fully contained into the single central slide, the adjacent channels show negligible impact (*Figure 5*).

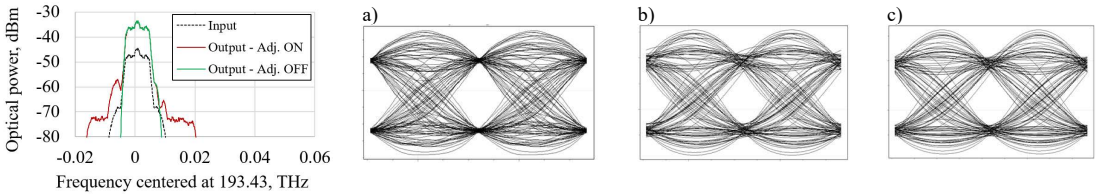

Figure 5: Signal spectra of the WBL 10 GBd input and output signals with eye diagram detail of a) the input signal, b) the output signal with adjacent slices on, and c) the output signal with adjacent slices off.

4. CONCLUSION

A monolithic WSS consisting of 4 identical WBL units has been presented. Each 64-λ WBL includes 11 MZIs, 16 AWGs, and 64 SOAs and has been investigated via hybrid time-and-frequency-domain simulations. The switching capability and impact of the selected component implementation is verified via the steady-state impulse response and large signal operation.

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