Single-chip Electronic-Photonic SoCs in a 45nm High-Volume CMOS Foundry: A Platform for Next-Generation Integrated Optics

Mark Wade
Ayar Labs, Inc., Emeryville, CA - USA
e-mail: mark@ayarlabs.com

ABSTRACT

Driven by relentless increases in high-performance ASICs (switches, GPUs, CPUs, DRAM, etc.), the electrical I/O roadmap is nearing its end, and the ASIC industry is looking for a ubiquitous replacement to electrical I/O escaping chip packages. To meet such demands, a photonics technology with massive bandwidth density, high energy efficiency, and low cost must be used. These requirements necessitate unprecedented levels of integration between electronics and photonics and require rethinking traditional communication architectures. In this talk, I will present a new class of optical devices integrated directly into a high-volume 300mm 45nm SOI CMOS process and how these devices enable new SoC's to solve the bandwidth bottleneck in the ASIC industry. Examples include a 400Gbps microring-based DWDM transmitter, a low latency RapidIO optical engine, and the first CPU chip with optical I/O.