

Photonic Integrated Circuit Platform using III-V on SiC Wafer

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Photonic integrated circuits (PICs) based on a high-index-contrast waveguide have paved a pathway to large-scale integration for photonics in the past ten years. Similar to Si photonics, we have investigated III-V CMOS photonics platform based on III-V on insulator (III-V-OI) wafer as shown in Fig. 1(a) [1]. We are able to fabricate ultrasmall InP PICs owing to the high-index contrast between III-V layers and SiO₂ buried oxide (BOX). Like Si-on-insulator (SOI) wafers, III-V-OI wafers can be fabricated by using direct wafer bonding [2]. Thus, we have demonstrated various passive components based on InGaAsP strip/rib waveguides including micro bends [2], arrayed waveguide gratings [2], and grating couplers [3]. Active components including modulators/switches [4], laser diodes (LDs) [4, 5], photodetectors [6, 7], and variable optical attenuators [8] have also been reported so far.

While the III-V-OI structure provides significant impact on device miniaturization for InP photonics, its low thermal conductivity is one of the drawbacks particularly for LDs. When free carriers are injected into an InP-based waveguide on the III-V-OI wafer, heat generated by current injection hardly dissipates through the thick SiO₂ where the thermal conductivity is quite low. Thus, the maximum power emitted from a single LD is limited to a few mW when its cavity length is approximately 100 μm [4]. Moreover, the poor thermal dissipation restricts the density of active devices on a single chip.

In this paper, we propose to use a SiC BOX instead of SiO₂ as shown in Fig. 1(b). Since the thermal conductivity of SiC is more than 100 times greater than that of SiO₂, we expect that the heat dissipation can be improved drastically by introducing a III-V on SiC wafer. On the other hand, the medium refractive index contrast between III-Vs and SiC arises concern about device miniaturization. Here we numerically analyze an InGaAsP waveguide on SiC in terms of bend loss and heat dissipation for feasibility study.

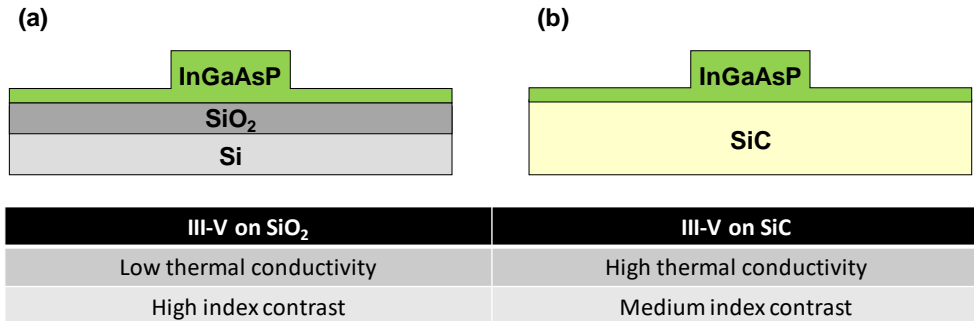


Fig. 1. Schematic of InGaAsP rib waveguide on (a) conventional III-V on insulator wafer and (b) III-V on SiC wafer proposed in this paper.

First, we evaluated the propagation loss of a 90° bend using 3D FD-TD simulation. Figure 2(a) is a comparison of bend loss of a Si strip waveguide on SiO₂ and InGaAsP strip waveguide on SiC as a function of the bend radius. While the medium index contrast of the InGaAsP on SiC waveguide resulted in the larger bend loss than that of the Si waveguide with the small bend radius, the difference in bend loss was negligible when the bend radius was greater than 7 μm, which is sufficient for large scale integration in most of PICs. Then, we analyzed the heat dissipation in the III-V on SiO₂/Si and III-V on SiC wafers as shown in Fig. 2(b). It was found that the increase in the device temperature of the III-V on SiC was 30 times smaller than that of the III-V on SiO₂/Si. Thus, the III-V on SiC platform enables large scale integration and high-power operation simultaneously.

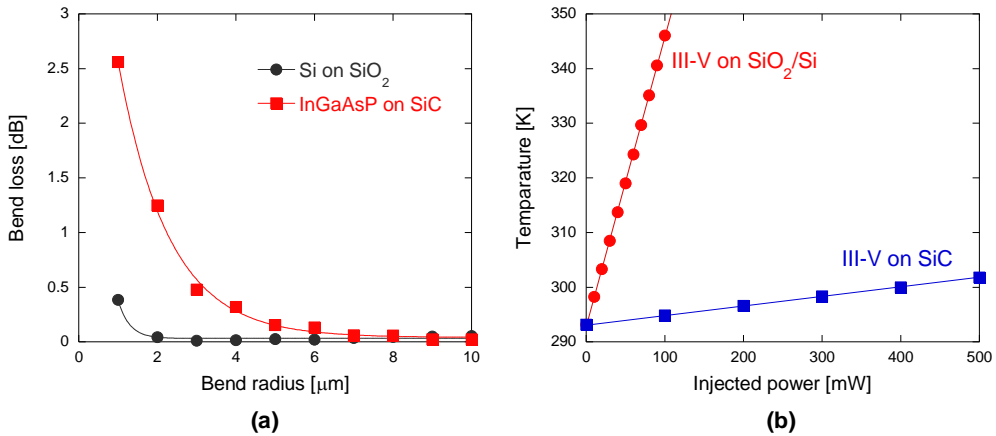


Fig. 2. (a) Bend loss of InGaAsP strip waveguide on SiC and Si strip waveguide on SiO₂ and (b) device temperature with injected power into III-V rib waveguide on SiO₂ and SiC.

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