EUROPEAN CONFERENCE ON INTEGRATED OPTICS

Silicon Photonics based WDM Systems: Chip and Module Level Integration

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The implementation of compact, dense WDM transceivers in Silicon Photonics (SiP), that are sufficiently cost and power efficient for Data Centre applications, is a notably challenging endeavour. Semiconductor Mode Locked Lasers (MLL) [1] and Resonant Ring Modulators (RRM) [2, 3] have been proposed as key devices for an elegant and efficient transceiver architecture. In recent works, we have shown that single section passively mode-locked MLLs can generate adequate optical carriers for 14 Gbps and 25 Gbps serial communications with on-off keying modulation [4]. A systematic analysis of the optical power budget of a solution comprising a MLL, an array of RRMs driven by hybridly integrated chip-scale electronics, and a Semiconductor Optical Amplifier (SOA) has also been reported [5]. At the 2017 European Conf. on Integrated Optics we will be reporting on recent progress towards integration of this transceiver architecture.

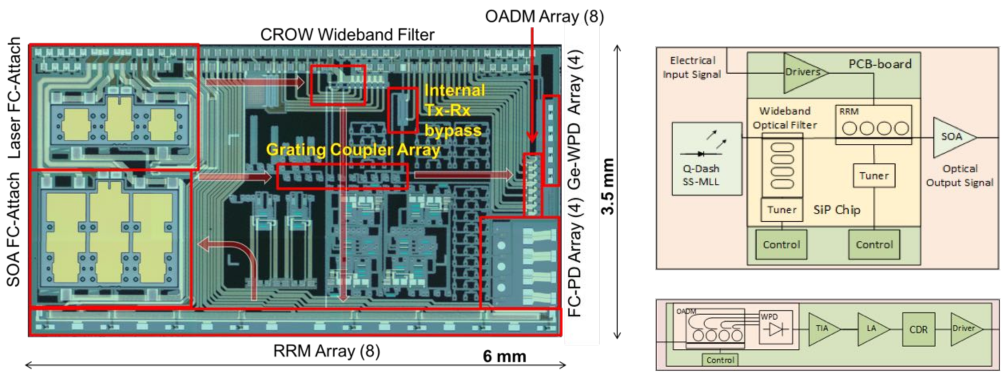


Fig. 1. Micrograph of the system chip and diagram of system architecture.

Fig. 1 shows a micrograph of the system chip as well as a block-diagram of the system architecture. A wideband optical filter implemented with coupled ring resonators in Coupled Resonators Optical Waveguides (CROW) configuration selects the highest power lines of the MLL as optical carriers for downstream modulation. Extinction of unused lines is essential to limit SOA saturation and the ensuing data distortion.

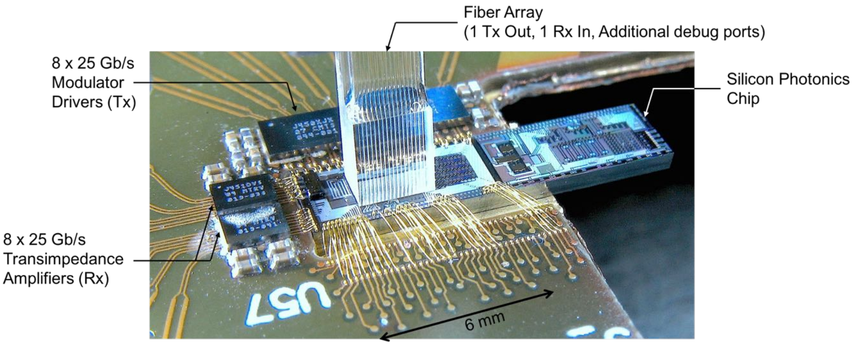
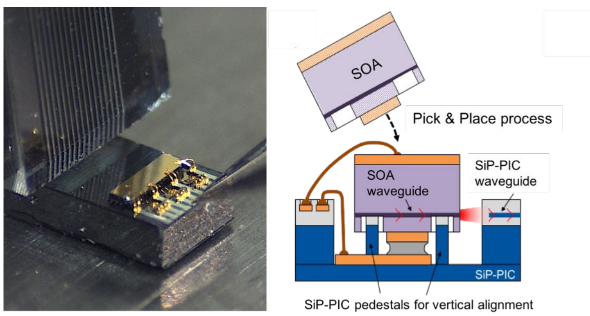


Fig. 2. Photograph of the SiP chip wire bonded to chip scale driver and receiver electronics. The MLL is coupled in by means of a lensed fibre edge coupled to the chip (not shown). The SOA is an external commercial device interposed between the Tx Out and Rx In ports.

Fig. 2 shows the currently evaluated transceiver, in which MLL and SOA remain external devices. We are currently building a demonstrator packaged as a module with flip-chip integrated MLL and SOA. To this end, we have developed a flip-chip integration process (Fig. 3) in which the vertical alignment is guaranteed by a mechanical contact between pedestals defined in a recess etched into the SiP chip and the laser or SOA [6]. We have introduced the extra refinement that the pedestal height is defined by selectively removing the SiP waveguide layer on top of the pedestals, and that corresponding mechanical contact areas are defined on the III-V chips by a selective wet etch stopping on top of the III-V waveguide layer. This way, the accuracy of vertical alignment is independent on the process control exerted on layer thicknesses during SiP or III-V chip fabrication. Horizontal alignment tolerances can be further relaxed with suitable edge couplers [6,7].



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