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A multi-channel photonic integrated transmitter driven by an application specific integrated circuit

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The dynamically developing market of modern fiber-optic access networks calls for high-speed, multi-channel photonic transmitters and receivers, technologically suitable for volume production at low cost. Such devices can be potentially developed using cutting-edge photonic integration technologies. At present, one of the major obstacles for broad implementation of photonic integrated circuits on the market are packaging constraints, especially related to providing many electrical RF interfaces. In this work we demonstrate and discuss a concept of hybrid integration of a multi-channel photonic integrated transmitter driven by an electronic application specific integrated circuit (ASIC). The two circuits will be bonded using a standard flip-chip technology. Such a hybrid integration scheme can provide an efficient method of driving multi-channel photonic integrated devices at high speed. To the best knowledge of the authors, such a concept is presented for the first time.

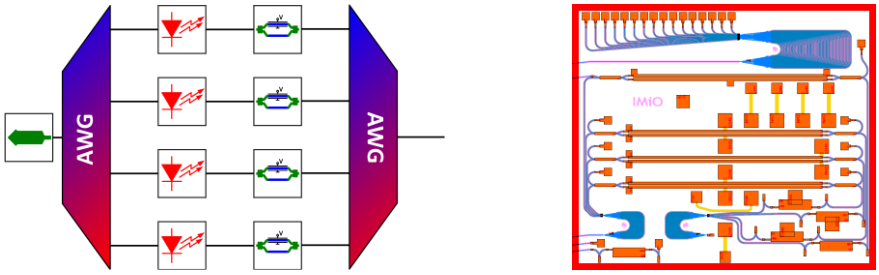

Fig. 1. The scheme of the four-channel photonic integrated transmitter and the mask layout of the photonic chip.

Fig. 1. presents the scheme of the realized photonic transmitter. It comprises four Fabry-Perot lasers constructed from a semiconductor optical amplifier and two-port multi-mode interference reflectors [1]. The lasers use filtered-feedback technique that enables single-frequency operation [2]. Filtering is provided by a 1×4 arrayed waveguide grating (λ_c = 1550 nm, $\Delta\lambda$ = 3.2 nm) and an MMI reflector. The lasers outputs are connected to

Mach-Zehnder modulators. The second AWG, with the same spectral properties as the filtering component, multiplexes four digital signals to a single chip output. The chip has been designed and fabricated in the generic process of SMART Photonics [3] – the mask layout (dimensions 4.6 mm × 4.0 mm) is presented in Fig. 1.

The application specific integrated circuit has been designed as an electronic driver of the photonic transmitter – DC supply for Fabry-Perot laser and digital signals for Mach-Zehnder modulators. The ASIC consists of three different wideband drivers and biasing circuits. It has been implemented and prototyped in the AMS 0.35 µm CMOS technology.

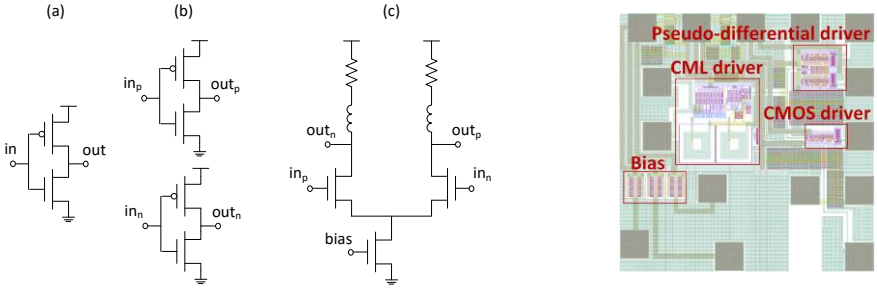

Fig. 2. Simplified schematics of: CMOS driver (a), pseudo-differential driver (b), current mode logic CML driver (c) and the ASIC chip layout.

The Mach-Zehnder modulators have two electric inputs, whose input impedance is capacitive. Measured capacitance of the modulators is around 4 pF. Fig. 2 shows simplified schematics of three different capacitance drivers that were implemented: a CMOS driver (a), a pseudo-differential driver (b), and a common mode logic CML [1] driver (c). The drivers (a) and (b) provide high output amplitude (rail to rail) and require small chip area. In the case of a simple CMOS buffer one of the modulator inputs is biased by a constant voltage. The driver (c) allows to achieve a higher bandwidth, but with a smaller output swing. To further increase the bandwidth of CML driver the inductive peaking technique [5] was used. Simulations show that the (a) and (b) drivers achieve 1.5 GHz bandwidth and CML drivers bandwidth is around 3 GHz, while driving 5 pF load.

The layout of the designed ASIC is presented in **Error! Reference source not found.**. The total chip dimensions are 2 mm × 2 mm. Big bonding pads (200 µm × 200 µm) visible on both the photonic and microelectronic chip will be used for flip-chip bonding of the two devices. Flip-chip technique will help to minimize the parasitic inductance and capacitance of the interconnection between ASIC and ASPIC.

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