Balanced Waveguide Avalanche Photodetector Chip

Tobias BECKERWERTH, Gan ZHOU, Sten SEIFERT, Angela SEEGER, Patrick RUNGE, Martin SCHELL
Fraunhofer Heinrich Hertz-Institute, Einsteinufer 37, 10587 Berlin

Abstract: We demonstrate a balanced waveguide avalanche photodiode chip with high bandwidth, sensitivity, linearity and low polarization dependence over the entire C-band. Moreover, we emphasize the integration with a homodyne coherent receiver for coherent transmission in data-centers.

1. Introduction

The worldwide internet traffic is still growing and short-haul transmission in intra- (0.5 to 2km) and inter-data center (<80 km) traffic covers more than 70% of overall traffic volume [1]. This raises the demand of optical-networks and therefore photodetectors which fulfill high sensitivity reducing the power consumption and also linearity for operation at higher modulation formats has to be achieved. For these specifications balanced avalanche photodetectors in a homodyne setup seem a suitable solution since avalanche photodiodes have proved to fulfil the requirements even for 100-Gb/s ethernet applications [2].

The presented balanced avalanche photodiode realizes good linearity as well as high output power and bandwidth above 20 GHz. This shows the potential for 28 Gbaud transmission systems. A conceptual setup of a homodyne receiver using two balanced APD chips is presented.

2. Design and Fabrication

The fabricated balanced APD is designed by using a SACM structure including a partially p-doped absorber region. The absorbing region consists of InGaAs while the multiplication and charge layer material is InAlAs [3,4]. The layer structure was grown on a waveguide lattice matched to InP using MOVPE on a 3-inch wafer. Furthermore, the balanced photodetector chip includes two single mode fibre spot-size converters and an integrated electrical bias network consisting of integrated capacitors and resistors.

3. Measurement Results

The photodetector chip is characterized by measuring the DC performance including gain and intrinsic responsivity but also the RF performance in terms of bias dependent bandwidth and linearity independently for each photodiode. In Fig.1 the measured dark current, photocurrent and resulting gain characteristics are presented. It shows a gain up to M=14 while the reverse bias voltage is not higher than 16 V. At unity gain voltage U_{M1}= 8.5 V the responsivity is higher than R > 0.60 A/W over the entire C-Band with a dark current lower than 10 nA (Fig.1). Additionally, the PD shows low polarization dependency where the PDL is

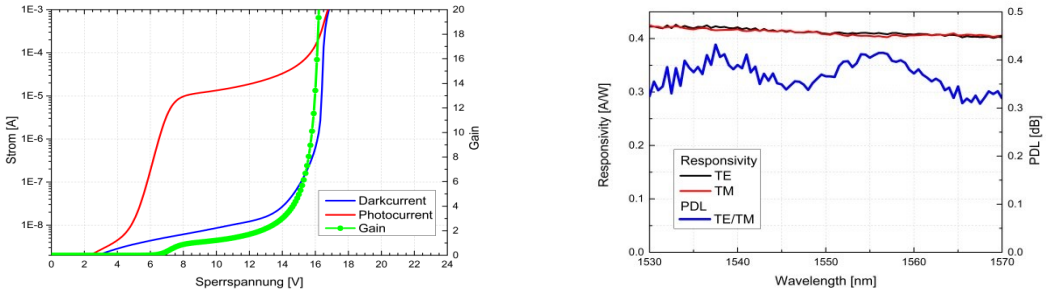

Fig. 1 UI-characteristics (left) and responsivity (right) of fabricated APD chip

below 0.5 dB. The f_{3dB} bandwidth as well as the linearity was measured separately on chip level applying different bias voltages U corresponding to different gains. The bandwidth (Fig.2) is up to f_{3dB}=24 GHz for low

gain at U=12 V and decreases with increasing bias voltage. For a gain up to M=5.5 at an operation voltage of U=15V the resulting bandwidth is still f_{3dB}=20 GHz for both APDs being sufficient for 28 Gb/s. At a higher gain up to M=14 a f_{3dB} bandwidth of 17 GHz is obtained.

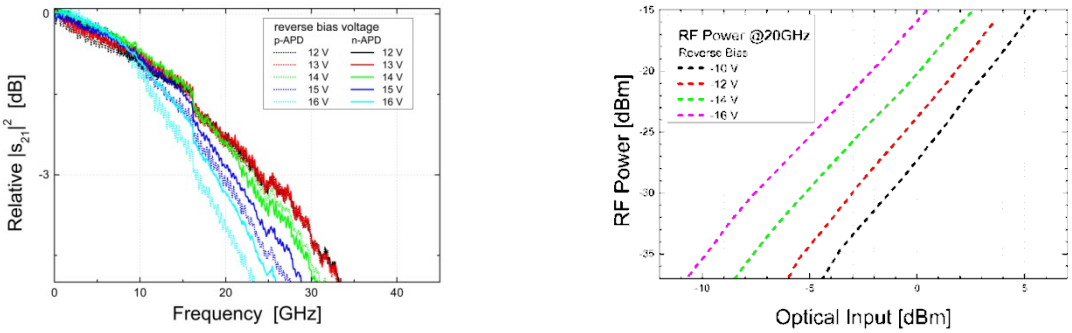

Fig.2 bias dependent bandwidth (left) and linearity measurement (right) of balanced APD chip

This results in a maximum gain-bandwidth-product of GBP = 238 GHz and responsivity-bandwidth product of 147 A/W GHz. The linearity of the chip was determined by varying the input power and measuring the RF ouput power at 20 GHz of frequency (Fig.2). A good linear behavior for input powers in the range of -10 to 5 dBm can be observed. As a result, the chip can detect higher modulation formats. A possible setup to use the chip for homodyne detection is proposed in Fig.3. Therefore, the same platform as in [5] can be used and the local oscillator (LO) is replaced by a delayed input signal. Due to the use of balanced photodiodes the difference of photocurrents can be obtained directly. In that way the overall power consumption of the receiver circuit is additionally reduced.

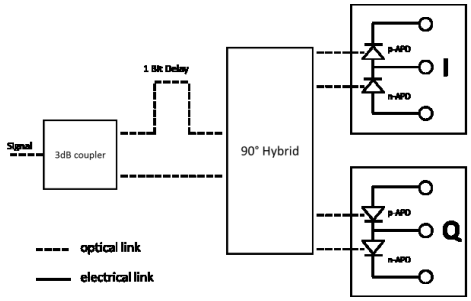

Fig. 3 Conceptual circuit model of homodyne receiver using balanced APD chips

4. Conclusion

A waveguide integrated balanced APD chip with high sensitivity and good linearity was demonstrated showing a bandwidth of 20 GHz at an overall responsivity of R=3.2 A/W and a SNR above 100. The high sensitivity, output power and linearity fulfill all demands for coherent receiver at 28Gb/s. With a homodyne setup the LO can be eliminated and when biasing the detector below U=16V even power consumption and heating can be reduced. First results on for O-band show low polarization dependence and even higher responsivity than in the C-band which all in all makes it a good candidate for data center applications.

[1] C. Xie, "Optical Interconnects for Data Centers",2016 IEEE PHOTONICS CONFERENCE, 29th Conf. of the IEEE Photonics Society (Waikoloa Village, USA, Octobre 2-6, 2016)

[2] M. Nada, "Vertical illumination InAlAs avalanche photodiode for 50-Gbit/s applications", 26th Int. Conf. on Indium Phosphide and Related Materials (Montpellier, France, May 11-15, 2014)

[3] J. C. Campbell, *Fellow, IEEE*, *Recent Advances in Avalanche Photodiodes,* JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 34, NO. 2, JANUARY 15, 2016

[4] S. Shimizu, K. Shiba, T. Nakata, K. Kasahara and K. Makita, "40 Gbit/s waveguide avalanche photodiodewith p-type absorption layer and thin InAlAs multiplication layer", ELECTRONICS LETTERS 12th April 2007 Vol. 43 No. 8

[5] P. Runge, "80 GHz Balanced Photodetector Chip for Next Generation Optical Networks" ,Optical Fiber Communication Conference 2014**,** (San Francisco, USA, 9-13 March, 2014)