

Silicon photonics: from present status to future developments

Piero ORLANDI^{1*}, Marco PIAZZA¹, Luca MAGGI¹, Antonio CANCIAMILLA¹
Giuseppe CUSMAI¹, Matteo TRALDI¹, Charles BAUDOT², Antonio FINCATO³

¹STMicroelectronics Agrate, Via Camillo Olivetti 2, Agrate Brianza, 20864, Italy

²STMicroelectronics Crolles, Rue Jean Monnet 850, Crolles, 38920, France

³STMicroelectronics Castelletto, Via Tolomeo 1, Cornaredo, 20010, Italy

* piero.orlandi@st.com

Silicon photonics gathered a great amount of investments during the last decade. Both research centres and major industries directed their resources towards this promising technology. As a result, different technological platforms have been proposed [1- 7] and some of them are now accessible through multi-project wafer services. This interest was fuelled by the idea of exploiting CMOS fabs capability to implement a large scale industrialization of low cost and highly integrated electro-optic chips. The amount of digital data exchanged is in fact constantly increasing: by the end of 2020 global IP traffic will reach 2.3 ZB per year, growing at a compound annual growth rate (CAGR) of 22% [8]. This trend is pushing the need for high data-rate optical communication systems toward shorter and shorter distances, from intra-data centers to on-board and on-chip communications [9]. Silicon photonics is seen as the most promising technology to reach the required cost per bit and level of integration and nowadays its evolution is mainly driven by the data centers market.

In this scenario, STMicroelectronics has developed an industrial silicon photonics platform in a 300 mm manufacturing facility [1]. The photonic technology, named PIC25G, employs 193 nm lithography and has been optimized to maximize the performance of passive and active photonic components of the Photonic Integrated Circuit (PIC). Particular attention has been posed to 1310nm and 1490nm wavelength ranges but also the transmission around 1550 nm is supported. The Electronic Integrated Circuit (EIC) is fabricated with a separate process and then flip-chip assembled to the wafer through copper pillars (see Fig. 1a). This choice allows to optimize both technologies separately, giving maximum design flexibility and minimal degradation with respect to fully integrated solutions.

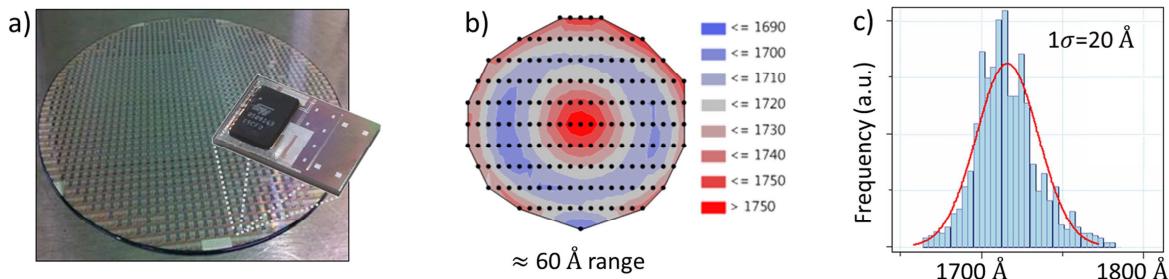


Fig. 1. (a) EIC die to 300 mm silicon photonics wafer assembly; (b) within-wafer remaining silicon thickness; (c) wafer-to-wafer remaining silicon thickness statistic.

Both PIC and EIC are tested separately at wafer level before assembly, using for both a fully automatic 300 mm compatible electro-optical probing station. This feature, fundamental for large scale industrial production, is enabled for the PIC by grating couplers. After the assembly of EICs on the PICs wafer, an Electro-Optical Wafer Sorting (EOWS) is finally performed with the same tool.

To ensure performance repeatability and uniformity of the devices at wafer level, a fine control of all the process steps is fundamental. For instance, focusing on grating couplers definition, silicon etching is the most critical step. PIC25G process control gives a within-wafer remaining Si thickness variability range of 6 nm (see Fig. 1b) while the wafer-to-wafer standard deviation is about 2 nm (see Fig. 1c). This process control allows a peak wavelength dispersion of grating coupler with a $\sigma \sim 2.4$ nm, able to guarantee strict specifications required by field applications. The SEM and TEM images of some of the active and passive devices developed in PIC25G are reported in Fig. 2. This set of devices, together with fundamental passive building blocks such as bends, multi-mode waveguides, tapers, directional couplers, and Y-junctions, forms a complete photonic technological platform, allowing to realize complex photonic integrated circuits. STMicroelectronics silicon photonics platform enables the fabrication of multi-channel transceivers with aggregate data-rate of 100 Gbps and beyond [1]. Transmission of non-return to zero (NRZ) modulated signals at 25 Gbps and 56 Gbps per-lane has been recently demonstrated with lower power consumption with respect to the state-of-the art [10].

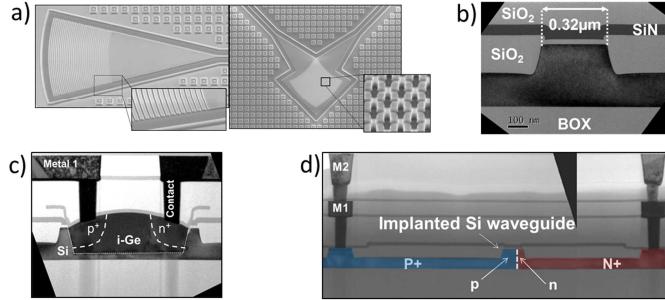


Fig. 2. (a) SEM top view of single polarization and polarization splitting grating couplers. TEM cross section of (b) single mode waveguide (c) photodiode and (d) PN junction based phase modulator.

In order to enable a fast, safe and product-oriented design, all the devices developed are included as building blocks in process-dedicated libraries within a Product Design Kit (PDK). The PDK provides an integrated environment for schematic-level photonic circuit design, circuit mask layout generation and performances simulations based on devices accurate modelling. The PDK also provides automatic check decks as Layout Versus Schematic (LVS) and Design Rules Checker (DRC), assuring compliancy with process design rules, a key point to guarantee manufacturability. Finally, the possibility of a full co-simulation of electrical and optical devices and circuits in 3D configuration is also included.

The next step for Silicon Photonic transceivers is addressing Wavelength Division Multiplexing (WDM) transmission systems. In order to move towards this kind of applications, a key element is the introduction of devices enabling for multi-wavelength management (Mux/DeMux). When the number of channels to be handled is low (i.e. 2, 4), Mach-Zehnder-based lattice filters [11, 12] represent the best solution to obtain low-loss and flat-band filters. However, in order to allow performance control and repeatability to maintain a high-yield, the design needs to be optimized minimizing sensitivity to process tolerances. The device has been fully engineered to achieve this task. Waveguide cross section has been optimized by using multi-mode waveguides for filter delay lines [11] and geometry of the single stage is engineered in order to minimize optical path lengths. Fig. 3a shows the measured response of a ninth-order filter designed to separate two channels compliant with the Coarse WDM grid requirements.

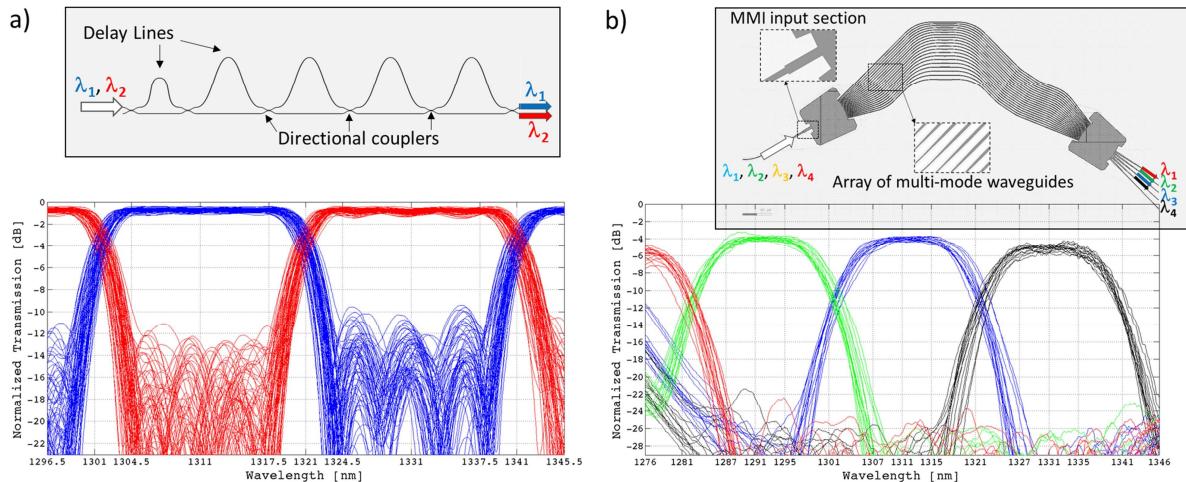


Fig. 3. (a) Measured transmission of 65 replicas (over different wafers) of a ninth order lattice filter. (b) Measured transmission of 20 replicas (over different wafers) of an AWG. Note that all spectra have been normalized by the means of reference grating couplers.

The measurements of 65 replicas of the same device (over different 300 mm wafers) are superimposed in the picture to highlight the good performance and the high repeatability obtained. Considering a channel bandwidth of 13 nm, the maximum Insertion Loss (IL) varies from 0.6 dB to 1.5 dB, with a median value of 1 dB, while the minimum Cross Talk (XT) varies from 8.4 dB to 16 dB, with a median value of 11.8 dB. A straightforward technique to achieve XT values usually required to fulfil system-level specifications, is to cascade the same filter as in [12]. This allows in fact to double the XT at the price of doubling the IL. When a larger number of channels has to be handled and a smaller footprint is required, Arrayed Waveguide Gratings (AWGs) are usually the preferred solution. Employing again multi-mode waveguides to reduce fabrication tolerance sensitivity, we designed and fabricated an AWG working on the CWDM grid with flattened band as in [13]. In Fig. 3b the measured spectra of the same AWG over 20 chips on different 300 mm wafers are reported. As for the lattice filter case, good performance repeatability is obtained. We demonstrated band flattening, 4.0

dB IL, 10nm -1dB bandwidth and 20 dB Crosstalk.

The reported results demonstrate that silicon photonics technology can play a role also for WDM applications in the near future. A future where, in order to keep up with the needs for larger aggregate bandwidths, also transmissions at higher bit-rates per lane (e.g. 56 Gbps) and with advanced modulation formats (e.g. PAM and QAM) will have to be provided. In order to implement novel functionalities, the development of new basic components and the improvement of the platform technology are required. The potential of silicon photonics can be enhanced by adding different active and passive optical materials through hybrid or monolithic integration [14]. Promising results have been recently shown in literature [15, 16]. Once the solutions most suitable for the chosen applications will be identified and selected, the main challenge will be reaching the requirements of the large volume production: high yield, efficient testing and sustainable supply chain.

Acknowledgments

The contribution of Antonio Fincato and Charles Baudot to this work was partially supported by the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 318178-PLAT4M

References

- [1] F. Boeuf *et al.*, *Silicon Photonics R&D and Manufacturing on 300-mm Wafer Platform*, Journal of Lightwave Technology vol. 34, pp. 286-295, 2016
- [2] S. Assefa *et al.*, *A 90nm CMOS integrated Nano-Photonics technology for 25Gbps WDM optical communications applications*, In International Electron Devices Meeting, San Francisco, CA, pp. 33.8.1-33.8.3, 2012
- [3] http://www2.imec.be/be_en/services-and-solutions/silicon-photonics.html
- [4] L. Zimmermann, *Monolithic Electronic-Photonic Co-Integration in Photonic BiCMOS*, In Proceedings of 42nd European Conference on Optical Communication (ECOC), Dusseldorf, Germany, W3F5, pp. 1-3, 2016
- [5] D. J. Shin *et al.*, *Integration of silicon photonics into DRAM process*, In Proceedings of Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), Anaheim, CA, OTu2C.4, pp. 1-3, 2013
- [6] D. Feng, B. J. Luff, S. Jatar and M. Asghari, *Micron-scale silicon photonic devices and circuits*, In Proceedings of Optical Fiber Communication Conference and Exposition (OFC), San Francisco, CA, Th4C.1 pp. 1-3, 2014
- [7] B. Szelag *et al.*, *Multiple wavelength silicon photonic 200 mm R&D platform for 25Gb/s and above applications*, In Proceedings of the SPIE, vol. 9891, pp. 98911C (15 pp.), 2016
- [8] CISCO White Paper, *The Zettabyte Era: Trends and Analysis*, July 2016
- [9] M. Zuffada, *The industrialization of the Silicon Photonics: Technology road map and applications*, In Proceedings of the European Solid-State Device Research Conference (ESSDERC), Bordeaux, pp. 7-13, 2012
- [10] E. Temporiti *et al.*, *Insights Into Silicon Photonics Mach-Zehnder-Based Optical Transmitter Architectures*, IEEE Journal of Solid-State Circuits, vol. 51, no. 12, pp. 3178-3191, 2016
- [11] F. Horst *et al.*, *Cascaded Mach-Zehnder wavelength filters in silicon photonics for low loss and flat pass-band WDM (de-) multiplexing*, Optics Express, vol. 21, pp. 11652-11658, 2013
- [12] S. Dwivedi *et al.*, *Coarse wavelength division multiplexer on silicon-on-insulator for 100 GbE*, in Proceedings of the IEEE 12th International Conference on Group IV Photonics (GFP), pp. 9-10, 2015.
- [13] S. Pathak *et al.*, *Optimized Silicon AWG With Flattened Spectral Response Using an MMI Aperture*, IEEE Journal of Lightwave Technology, vol. 31, no. 1, pp. 87-93, 2013
- [14] <http://www.h2020-cosmicc.com/>
- [15] W. D. Sacher *et al.*, *Multilayer Silicon Nitride-on-Silicon Integrated Photonic Platforms and Devices*, IEEE Journal of Lightwave Technology, vol. 33, no. 4, pp. 901-910, 2015
- [16] T. Ferrotti *et al.*, *O-Band III-V-on-Amorphous-Silicon Lasers Integrated With a Surface Grating Coupler*, IEEE Photonics Technology Letters, vol. 28, no. 18, pp. 1944-1947, 2016