

Wavelength Locking Platform for 4×10 Gbit/s L-Band Si-Photonic Multiplexer and Carver

Andrea MELLONI^{1*}, Stefano GRILLANDA¹, Marco CARMINATI¹, Emanuele GUGLIELMI¹, Nicola PESERICO¹, Federica MAULÁ¹, Giorgio FERRARI¹, Antoine DENTIN², Alberto DEDÉ², Antonio BERETTA², Danilo NICOLATO², Marco CREATINI², Barry HOLMES³, Charalambos KLITIS³, Marc SOREL³, Shengmeng FU⁴, Ruiqiang JI⁴, Antonello VANNUCCI², Marco SAMPIETRO¹ and Francesco MORICETTI¹

¹Politecnico di Milano, Dip. di Elettronica, Informazione e Bioingegneria, 20133 Milano, Italy

²Linkra Microtech, 20864 Agrate Brianza, Italy

³University of Glasgow, School of Engineering, G12 8LT Glasgow, United Kingdom

⁴Fixed Network Research Department, Huawei Technologies Co., Ltd, 518129 Shenzhen, China

*andrea.melloni@polimi.it

Silicon (Si) photonics is a promising platform to satisfy the ever-increasing request for high-capacity, high-performance, low-cost and low-power consumption of high data-rates interconnections. Yet, Si circuits are extremely sensitive to parasitic effects such as manufacturing tolerances and thermal crosstalk, strongly limiting circuit complexity. Here, we demonstrate a wavelength locking platform enabling automatic feedback control of a Si photonic circuit performing multiplexing and carving of 4×10 Gbit/s wavelength division multiplexing (WDM) channels in the L-band.

Figure 1(a) shows a picture of the fabricated Si photonic circuit, integrating 4 microring resonators (MRRs). Each MRR resonance is suitably tuned with respect to the carrier wavelength of the *i*-th signal (Ch. *i*) in such a way that the 4 channels are multiplexed to the common bus waveguide and spectrally reshaped to enhance the signal extinction ratio (ER). Figure 1(b) shows a photograph of the realized demo board hosting the 4×10 Gbit/s WDM transmitter. The transmitter is composed by 4 indium phosphide-based packaged directly modulated lasers (DMLs) operating in the L-band, whose bias and modulation currents are provided by CW and radiofrequency drivers integrated

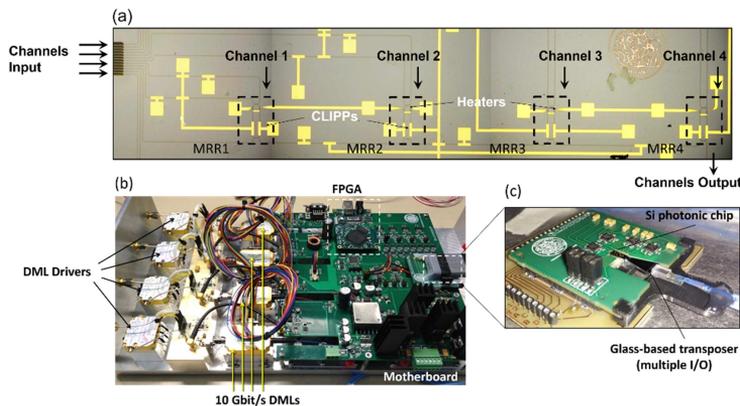


Fig. 53: (a) Top-view photograph of the fabricated Si photonic circuit; (b) Board hosting the 4×10 Gbit/s Si photonic transmitter; (c) Detailed view of the mini-board hosting the Si photonic chip and the glass-based transposer for multiple I/O.

onto the board. An FPGA is used to manage the wavelength locking of the MRRs to the DML signals. The Si chip is bonded to a glass-based transposer for multiple fiber input/output and is placed onto a printed circuit board (PCB) [Fig. 1(c)]. Automatic

tuning and feedback control of the 4 MRRs is realized by using thermal actuators integrated in the Si chip and ContactLess Integrated Photonic Probes (CLIPPs) to monitor the MRR resonances [1].

A sketch of the control system for each MRR is reported in Fig. 2(a). The MRR heater voltage is set according to an integral control law, employing as an error signal ε the ratio between the input power (CLIPP_{IN}) and that measured inside the MRR (CLIPP_{MRR}). Figures 2(b) and (c) show the eye diagram of the 10 Gbit/s DML signal respectively at the output of the DML and after the Si MRR. The DML is driven with a bias current of 60 mA and with a modulation depth of about 35%. The MRR has bandwidth 8 GHz and FSR = 124.5 GHz. The signal at the DML output (Q-factor = 3.6, ER = 2.6 dB) is transmitted through the MRR, that improves its quality by enlarging the eye aperture, thus achieving ER = 8.8 dB and a Q-factor of 4.2.

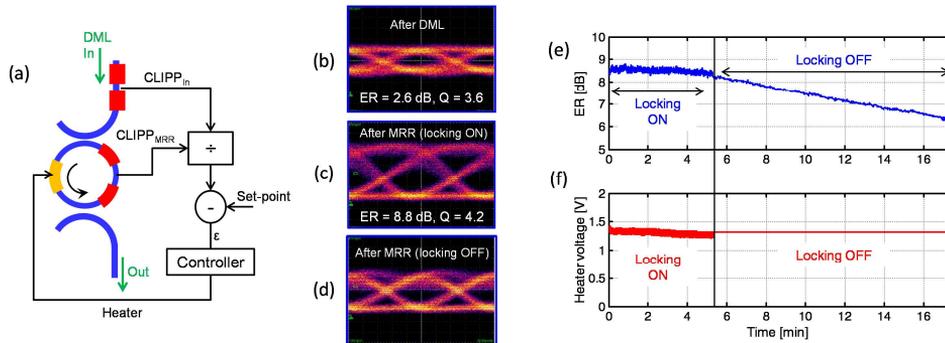


Fig. 54: (a) Wavelength locking scheme of each MRR of the Si photonic transmitter; 10 Gbit/s eye diagram (b) after the DML and after the MRR carver with the feedback control (c) ON and (d) OFF; (e) Extinction-ratio and (f) MRR heater voltage as a function of time when the locking is ON and OFF.

To test the effectiveness of the feedback system, the TEC of the Si chip was switched OFF, letting the MRR subject to ambient temperature gradients. Figure 2(e) and (f) report respectively the time-dependent ER of the signal after the MRR and the voltage applied to the heater, when the locking system is ON (time < 5 min) and OFF (time > 5 min). The corresponding eye diagrams of the signal after the MRR are shown in Figs. 2(c) and (d). Although the TEC of the Si chip is OFF, when the feedback control is active the eye aperture remains well open and the ER of the signal is stable around 8.8 dB [Fig. 2(c)] (Q-factor is about 4.2 dB). The beneficial effect of the feedback is confirmed when the locking system is switched OFF: the MRR wavelength drifts under the effect of the ambient temperature variations. As a consequence, the DML signal and the MRR drift apart, degrading the quality of the signal [ER down to 6.5 dB and Q-factor down to 3.5 as shown in Figs. 2(d-e)].

In conclusion, we have demonstrated automatic feedback control of a 4 × 10 Gbit/s WDM Si photonic multiplexer and carver on a wavelength locking platform enabling TEC-free operation without signal performance degradation.

[1] S. Grillanda et al., *Optica* 1(3), 129 (2014).