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Low-Energy, Dilated 4x4 Hybrid MZI-SOA Cross-point Optical Switch

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Optical switches are regarded as potential key enabling components for future communication routing systems to accommodate significantly increasing internet traffic in both data-centres and the core network [1]. Opto-electronic devices, such as semiconductor optical amplifiers (SOAs) and Mach-Zehnder Interferometers (MZIs), with nano-second response times have received much attention since they are able to fulfil the requirements of packet switching [2]. SOAs offer high ON/OFF extinction ratio and broadband operation. However, SOA-based switches are constructed using a broadcast-and-select architecture, where splitters/combiners introduce inherent loss. This loss is compensated for by the gain provided by SOAs, although this is accompanied by amplified spontaneous emission (ASE) noise and saturation-induced distortion. MZI-based switches avoid the inherent loss due to splitters/combiners but they suffer from poor crosstalk performance and exhibit insertion loss.

Therefore, we have proposed a novel hybrid MZI-SOA switch approach to utilise the advantages of both components [3]. As shown in Fig.1(a), the MZIs act as the switching elements and the SOAs are used to suppress the crosstalk signal in the OFF state and compensate the passive components' loss in the ON state. A 2×2 hybrid switch has been reported in [4], which shows 26 dB input power dynamic range (IPDR) for a power penalty of less than 0.5 dB. A rearrangeably nonblocking 4x4 hybrid switch can be built by connecting the modular 2x2 blocks in a dilated Beneš architecture [Fig. 1(b)].

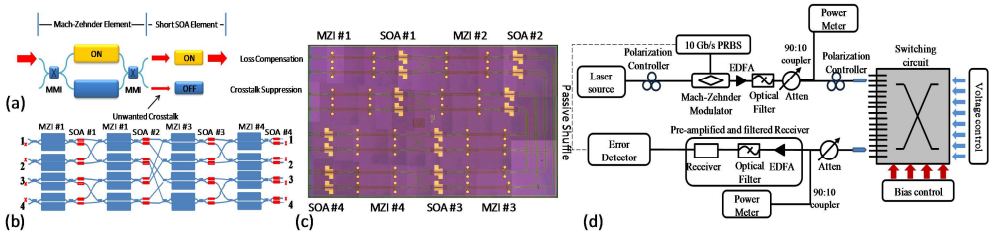

Fig. 34. (a) Operating principle (b) Schematic of a 4x4 switch (c) Photograph of the fabricated 4x4 switch (d) the experimental test-bed.

Fig. 1(c) shows the fabricated 4x4 switch chip produced within the EU FP7 PARADIGM project [5]. The chip is realised within a multi-project wafer run with generic basic building blocks based on the InGaAsP material system and has a size of 4 mm × 6 mm. The limited chip size requires the layout to be folded to fabricate all the elements as shown in Fig. 1(b). Each path on the switch contains four 1000/900 μm long MZIs and 230/250 μm long SOAs. The 250 μm long SOAs are used before the passive shuffle network in order to compensate for excess loss. The input and output facets of the chip are anti-reflection coated.

The static characteristics of the longest path are measured using the test-bed shown in Fig. 1(d). The switch is mounted on a thermo-electric cooler and maintained at 20 °C.

Lensed fibres are used to couple light into/out of the chip. The gain performance of the SOAs is characterised by determining their transparency current, which is found to be 3.7/4.2 mA for the 230/250 μm long SOAs respectively. The passive loss of the path can be measured when all SOAs are biased at transparency. The power budget of the longest path through the switch is shown in Fig. 2(a), with the components listed as follows: S-bends (S-Bs), multimode interference couplers (MMIs), phase modulators, semi-circular bends (SC-Bs). The 1000/900μm MZIs exhibit 2.2/2dB insertion loss respectively. 15/17 mA bias currents are chosen for the 230/250μm SOAs respectively to ensure lossless operation. The switch exhibits a peak gain at 1535 nm with a 3 dB bandwidth of 22.5 nm. The switch exhibits more than 100dB ON/OFF extinction ratio.

BER measurements are performed at a wavelength of 1535.89 nm. The optical input to the switch is generated by a tuneable laser that is modulated by a Mach-Zehnder modulator driven by a 10 Gb/s 2^{31}-1 pattern length PRBS. The output is connected to an optically pre-amplified and filtered receiver and an error detector. Fig 2(b) shows the power penalty at a BER of 10^{-9} versus the on-chip input power. The 0.5 dB-penalty IPDR exceeds 15 dB. Each path consumes electrical power of 6 2mW and the energy consumption per bit is 6.2 pJ at a 10 Gb/s data rate, featuring a 42% lower energy consumption compared to equivalent 4x4 SOA switches [1].

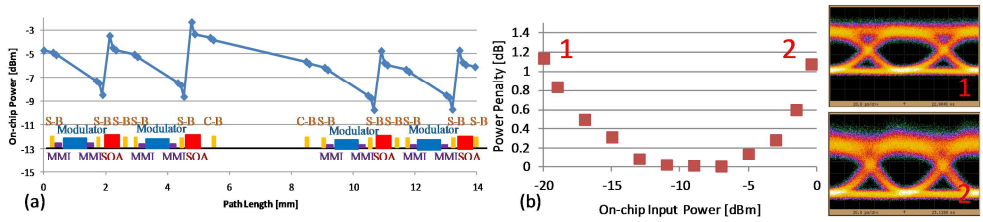

Fig. 2. (a) Power budget for the longest path (b) IPDR curve with eye diagrams measured at -20 and 0dBm on chip input power.

In conclusion, this paper presents the first integrated 4x4 hybrid MZI-SOA switch that offers lossless operation. The longest path exhibits more than 15dB IPDR for a penalty less than 0.5 dB.

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