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Fast and Energy Efficient Micro-Ring-Resonator-Based 4×4 InP Switch Matrix

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Wavelength-selective micro-ring resonators combined with electro-optic tuneable elements can provide fast switching functionalities. Most of the research done so far on active micro-ring resonators has however focused on the realization of first-order micro-ring resonator based devices such as filters and lasers [1-2] or on monolithically integrated switches on Silicon on Insulator (SOI) platform [3]. However, the inherent trade-off between the achievable bandwidth and the signal extinction in first-order micro-rings [4] have limited their use in switching. Moreover, nanoscale feature size variations lead to a shift of the peak wavelength of the same order [4] which particularly complicates applications in large scale circuits.

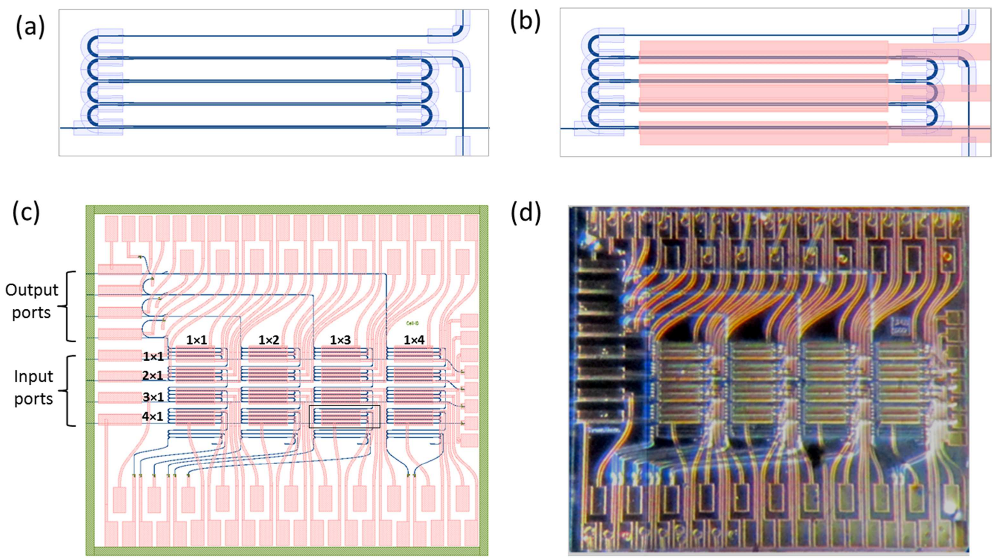

Fig. 32. (a) Single switching element composed of three race-track micro-rings. (b) Electrodes (in red) place on the top of directional coupler for fine tuning. (c) Full layout of the chip, including the optical wiring layer (in black) and the metal wiring (in red). (d) Photograph of the fabricated chip.

Higher-order resonator have been shown to decouple the trade-off between the bandwidth and the signal extinction so that both data bandwidth and switch speed parameters can be optimised together [5-6] This also enables an enhanced bandwidth of such devices and improves tolerance to variations in fabrication [4]. The possibility of achieving faster switching times and low power consumption makes III-V material platform very attractive for photonic integrated circuits based on ring resonators.

In this work, for the first time a 4×4 switch matrix based on higher-order resonant elements is designed and fabricated in the InP material platform. Third-order ring resonators (Fig. 1a) are designed and placed in a cross-point matrix. Fast electro-optic tuning is used to allow data to drop to the next port or pass through. Three electrodes per element are provided to allow the reciprocal tuning of each element (Fig. 1b). The full mask layout and a photograph of the realized chip are shown in Fig. 1c and d.

10Gbps data routing is performed across a combination of 4 different paths in the circuit. Furthermore, a representative path is used to demonstrate higher, passband-limited line-rate of 20Gbps (see Fig. 2a). A maximum power penalty of 2.6 dB is recorded. The on-state electrical power consumption is only 79 µW, which leads to an energy consumption of 8 fJ/s for 10 Gb/s operation. Fast switching of a few nanoseconds for the rise and the falling time is measured as shown in Fig. 2b.

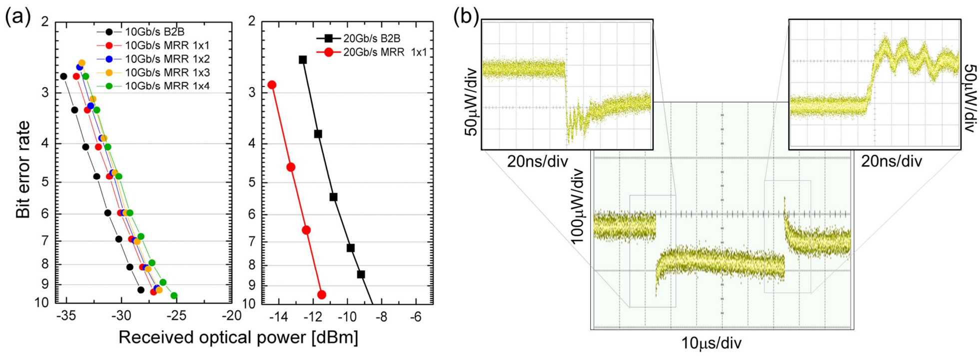

Fig. 33. (a) Bit error rate for 10 and 20 Gbps line rates. (b) Time traces for switching time: falling time in the left-hand side inset and rising time in the right-hand side inset.

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