Integrated Optical Switch Matrices

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Abstract: High connectivity integrated optical multi-stage switch matrices with up to sixteen input ports and sixteen output ports are demonstrated using active-passive integrated circuits. 192 switching active elements and hundreds of passive components are integrated within the same monolithic chip for establishing optical data connections at the packet time-scale. We trace circuit level performance through to component level design for even higher levels of connectivity.

Optical switching technology has been proposed to enable Terabit class data routing[1]. Integrated optoelectronics can however offer a radical reduction in physical size and avoids the considerable complexity at the circuit assembly stage. Further scaling requires sophisticated multi-stage networks.
Semiconductor optical amplifier (SOA)-based circuits offer the prospect of large-scale integration, broadcast, higher radix switch elements and the possibility to use multiple stages of loss-compensating switch elements. Bandwidths of up to 160 Gb/s have already been demonstrated through a multi-stage 4×4 optical switch[2]. Recently, feasibility studies and experimental work have shown that lossless 16×16 port count can be achieved using cascades of 4×4 devices in an all-active InP/InGaAsP wafer epitaxy[3,4], but the long all-active paths degrade the optical signal-to-noise ratio and requires high operating current.
In this work, we present and analyse active-passive optoelectronic 16×16 switch by monolithically integrating multi-stages of active SOA gate arrays with passive shuffle networks. This allows for loss compensation, lower power consumption, with reduced signal impairment.

16×16 optical switch matrix. A rearrangeably non-blocking switch is designed implementing a hybrid-Benes architecture[5]. The central five stages are collapsed to one stage by using a 4×4 broadcast and select switch architecture and the input and output switching stages are implemented with 2×2 broadcast and select switching elements. Fig. 1 shows a photograph of the switch circuit. Optical fiber connections are made via the facets at the top and bottom of the image. Electrical connections are made from the left and right sides. Bond wires are provided for the input and output switch elements, and also for one of the two planes of switch elements in the center stage.

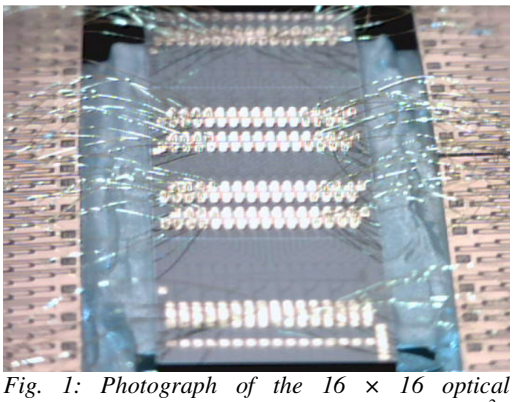

Fig. 1: Photograph of the 16 × 16 optical switching matrix. Chip dimensions are 4 × 14mm^2.

The three cascaded SOA gate stages are implemented across six columns of 30 μm wide and 500 μm long quantum well active islands on a selective area epitaxial regrown InP/InGaAsP wafer. The circuit is fabricated with an eight-mask process. The first waveguide mask defines the waveguide paths: the shortest path is 14 mm and the longest path is 19 mm. The shallow, deep, ultra-deep and electronically isolated waveguides are defined using four photolithographic masks. Inductively coupled plasma etch processing ensures a high side wall verticality to minimize polarization rotation[6]. Waveguide bends with radii as low as 20 μm are implemented in the first mask layer to ensure a compact circuit footprint. The second and third mask patterns define 1.7 μm wide deep-etched 100 μm waveguide bends and 2.2 μm wide shallow-etched straight-waveguides, respectively. The fourth pattern removes p-doped contact layers above the passive waveguides. Mode-matching from deep to shallow waveguides is performed using tapered waveguides. The circuit is planarized before metal evaporation and a lift-off process finally defines the separately addressed p-electrodes. Measurements are performed at 15°C on a temperature stabilized, water-cooled copper mount.

Performance. The switch matrix performance is characterized in terms of gain, loss and noise for paths from the extreme input ports 1 and 16 towards all 16 output ports. Gain and optical signal to noise ratio (OSNR) are initially measured for the enabled path input 1 to output 1 with varied SOA operating condition in Fig 2*a* and *b*.

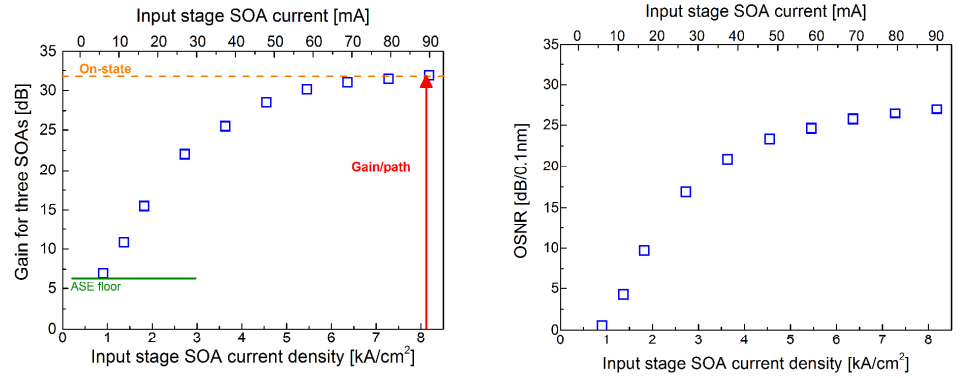

Fig. 2: Gain for three SOAs (a) and optical signal to noise ratio (b) for path 1 to 1 as a function of injected current at the input SOA. The central and output SOA currents are set at 90 mA and 160 mA, respectively.

The net chip gain for path input 1 to output 1 is obtained by normalising the fiber-to-fiber signal losses to the total passive losses of 60.1 dB. A total net gain of up to 10.6 dB per SOA is estimated from the combination of current dependent gain and the anticipated path losses[5]. This shortest path contains up to thirty-eight passive components, as well three active elements, for a net on-chip loss of -17.2 dB. This SOA gain is enough to compensate the inherent splitter losses of 30 dB. The longest paths contribute an additional 8.2dB excess loss due to additional twenty-four components and 5mm waveguide length. Optical signal-to-noise ratio is found to be as high as 28.3dB/0.1nm for the same SOA operating conditions.

To gain insight into circuit level performance, the optical signal to noise ratio is measured for the broad range of paths (Fig. 3). The loss variation per path also leads to a path dependent OSNR in the range from 13.7 up to 28.3 dB. The optical signal to noise ratio is predicted using the anticipated excess losses for the passive components[5], and the observed level of gain and ASE power spectral density from the on-state SOA gates. Excellent agreement is observed, except for the case of the paths from input 16 to output 9-12, due to two imperfectly resolved waveguides. The OSNR approaching 28.3dB/0.1nm already allow for 10Gb/s data routing[5]. The noise figure per stage are estimated to be 14.3, 9.2 and 10.6 dB for the input, central and output SOA, respectively, for a total circuit noise figure of 14.5 dB. These values are due to the low average input powers of -11.9, -21.1 and -36.1 dBm respectively at the first, second and third SOA stage. A considerable enhancement may be anticipated with lower excess losses for the passive components, bringing the circuit level noise figure down to 7.8 dB. This opens a route to further scalability.

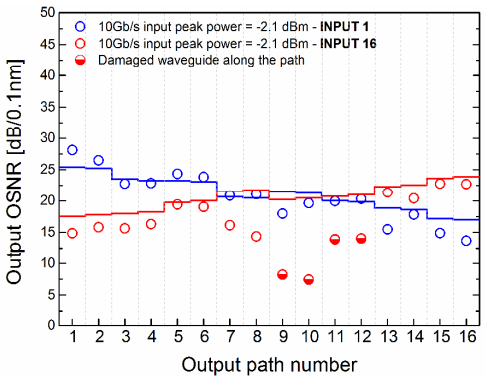

Fig. 3: Path dependent noise performance. Experiment (symbols) and prediction (solid lines).

References

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