Foundry based approach for InP based PIC development

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Abstract: The generic foundry model will reduce the R&D and prototyping costs and the throughput time of Photonic ICs by more than an order of magnitude. The concept of generic photonic integration is discussed and the current status and prospects of generic InP-based integration technology are reviewed.

In photonic integration most integration technologies are developed and optimized for a specific application. As a result we have almost as many technologies as applications, most of them very similar, but sufficiently different to prevent easy transfer of a design from one fab to another. Owing to this huge fragmentation, the market for many of these application-specific technologies is too small to justify their further development into a low-cost industrial volume manufacturing process. And as a result the chip costs remain too high to find wide application.

This is quite different from microelectronics where a huge market is served by a small set of integration processes (most of them CMOS processes). In these processes a broad range of functionalities can be realised from a small set of basic building blocks, like transistors, resistors, capacitors and interconnection tracks. By connecting these building blocks in different numbers and topologies we can realize a huge variety of circuits and systems, with complexities ranging from a few hundred up to over a billion transistors. We call such a process, in which a broad range of functionalities can be synthesized from a small set of basic building blocks, a ***generic integration process***.

In photonics we can do the same. An integration process with building blocks for controlling the basic properties of light: the amplitude, the phase and the polarisation, can support a broad range of functionalities. And by integrating these building blocks with a good waveguide structure we can make interconnections, but also passive components like couplers, filters and demultiplexers. With optical amplifiers (SOA: Semiconductor Optical Amplifier), phase modulators and polarisation converters, for manipulating the amplitude, the phase and the polarisation of the light, the technology can support a broad range of functionalities.

An advantage of generic integration technologies is that because they serve many different applications, they justify the investments in developing the technology for a very high performance and reliability at the level of the building blocks. This will make circuits realised in such a technology highly competitive. A single generic process will not be suited to all applications, of course. Just like in microelectronics we will need a few different generic technologies, optimized for different kinds of applications. But the number of generic technologies can be small, much smaller than the variety in today's technologies.

Such generic integration processes have been developed in the European projects EuroPIC and PARADIGM, and (Dutch) national projects like MEMPHIS, IOP Photonic Devices and STW Generic Technologies for Integrated Photonics. On these experimental platforms more than a hundred different Photonic ICs have been fabricated for applications in telecom, datacom, medical diagnostic, metrology, sensing and security.

Another advantage of a standardized technology is that we can develop design libraries and a related software infrastructure for components or subcircuits that are used by many designers. This leads to a significant reduction of the design time and an increase in the design accuracy, so that fewer design cycles will be necessary to arrive at a required performance.

An important advantage of generic integration technology is that a number of different designs can be combined on the same wafer, because they all use the same fabrication process. Such a wafer is called a Multi-Project Wafer (MPW). And the Photonic ICs fabricated in such an MPW run are called ASPICs: Application Specific Photonic ICs, the photonic equivalent of an ASIC. *ASPICs are application-specific PICs, realised in a standardized generic process*. This approach leads to a large reduction of the research and development costs. In the development stage often a few design and fabrication cycles are necessary to arrive at the required performance. Usually a few chips out of the wafer are sufficient for testing the design in this stage. By combining a number of designs on a single wafer every designer gets a few chips and the costs of the run can be shared by all participants in the MPW-run. This will lead to a more-than-ten-fold reduction of the costs of a design run.

If the owner of a generic integration process does not provide access to external users the number of companies that can take advantage of this approach remains restricted to a few companies that develop sufficient different products to make a generic approach profitable for themsleves. The corner stone of the generic foundry model is the generic foundry: a chip manufacturer that provides open access to its generic integration process(es). In silicon microelectronics a number of chip manufacturers are providing such foundry access. In Photonics a few companies and institutes have started providing semi-commercial access to generic foundry platforms.

The anticipated large reduction of R&D time and chip manufacturing costs will lead to a large growth of the share of PICs in the photonic components market. So far the commercial deployment of PICs has been mainly restricted to specific areas in telecom core-network applications, where their functionality cannot be matched by competing technologies. Telecom is a relatively niche area for the exploitation of photonic technologies, accounting for about 5% of the global photonics market. Nonetheless the stringent requirements of telecoms are driving PIC research. Thus the opportunities to leverage PIC technology in other established photonic markets such as fibre sensor readout units, medical diagnostic, metrology and many applications where today's photonics does not provide a competitive price level, are immense.

Another important advantage of the generic foundry approach is the short time-to-market. Because the ASPICs are developed in a qualified foundry process upscaling to larger production volumes is straight forward: once the ASPIC design meets the user requirements, the user can order a number of wafers in the same process in which he developed his ASPIC, which he can now fill completely with his design.

All this brings a fundamental change in the business model of photonics and allows commercial and academic groups to co-operate and move forward rather than forever reinventing the wheel.

In the presentation the present status of the InP-based generic foundry approach will be reviewed, and future developments in platform technology development, process design kits and component libraries, generic packaging and testing will be discussed.

References

M. Smit et al, “An introduction to InP-based generic integration technology”, accepted for publication in *J. of Semicon. Science and Technology, 2014.*