Towards a high bandwidth waveguide photodetector in an InP membrane on Silicon

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Abstract: An InP membrane based waveguide photodetector is designed to reach a 3 dB bandwidth beyond 100 GHz. A uni-traveling-carrier (UTC) configuration is used for minimizing the carrier transit time. A novel double-side process technology is developed to enhance the bandwidth. In addition, a low resistance n-type contact technology is optimized to control the metal spiking into semiconductors.

Introduction and design: InP Membrane on Silicon (IMOS) technology provides a new platform for integration of passive and active photonic devices on top of CMOS chips.[1] These devices are fabricated in an InP-based membrane which is bonded to a silicon wafer by using benzocyclobutene (BCB). Recently, a uni-traveling-carrier photodetector (UTC-PD) in the IMOS platform is being developed for high speed applications. The carrier transport in UTC-PDs is dominated by electrons due to the utilization of a p-type doped absorption layer.[2] The higher velocity of electrons compared to holes results in a higher bandwidth than in conventional PIN-PDs.

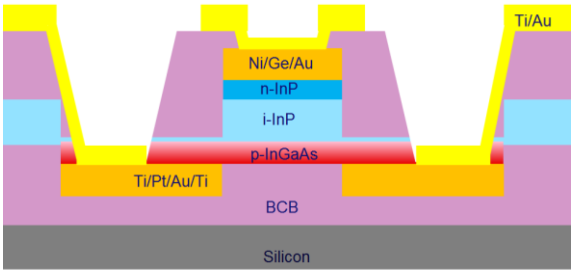

Fig. 1: Cross-section of the UTC-PD.

The designed structure is shown in Fig. 1. The width of the PD mesa is designed as 3 µm. A 300 nm thick intrinsic InP layer is used both as the passive waveguide and as the electron collector (depleted) in the UTC region. A 150 nm thick p-type doped InGaAs layer is used both as the absorber and the p-contact. This layer is doped with a gradient concentration from 10^{18} cm^{-3} at the collector-absorber interface to 10^{19} cm^{-3} at the contact surface. Optical simulation gives a modal absorption coefficient of 3600 cm^{-1} at 1.55 µm. This high absorption is due to the strong confinement of the optical mode in such a high index contrast membrane. The PD is designed to be 10 µm long, which is sufficient for an absorption efficiency of 97%. The small device area results in a junction capacitance of less than 10 fF.

The carrier transit time of a UTC-PD consists of two components: the electron diffusion time in the p-type InGaAs absorber, and the electron drift time in the depleted InP collector. The first term can be reduced below 1 ps with the doping gradient in the p-type InGaAs layer.[2] In terms of the electron drift time, UTC-PDs can be set with an optimal bias voltage so that electrons travel at the velocity overshoot (above 2×10^{7} cm/s).[2] At this bias, the electron drift time through the 300 nm collector is only 1.5 ps. The bandwidth limited by a total transit time of 2.5 ps is calculated to be 150 GHz.

Double-side process technology: While the transit time and the capacitance are minimized, the high sheet resistance of a thin membrane device remains the major limiting factor for the bandwidth. In order to reduce the series resistance of the p-contact layer, a double-side process scheme (Fig. 2) is used to evaporate the p-metal (Ti/Pt/Au) at the back side of the device before bonding to Si. In this way the spacing between p-metal can be made sufficiently narrow to minimize the series resistance. An optimized spacing of 3 µm (equal to the mesa width) is chosen as a trade-off between the metal loss and the resistance (Fig. 3). At this point, the metal loss (340 cm^{-1}) is very limited compared to the modal absorption (3600 cm^{-1}). The resistance is simulated by considering a conductivity of 9000 S/m and a specific contact resistance of 3×10^{-6} Ω cm^{2} of the InGaAs layer. In case of p-metal on top of the membrane (n-side, same side as the mesa), a practical limit from lithography determines the smallest

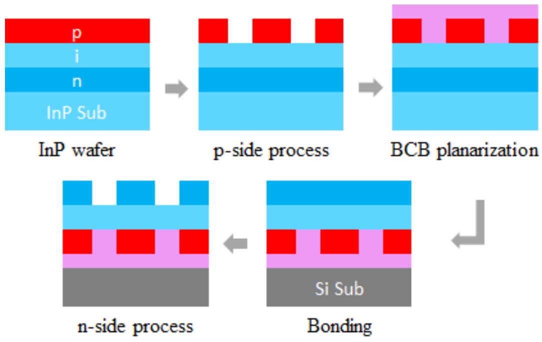

Fig. 2: Overview of double-side process.

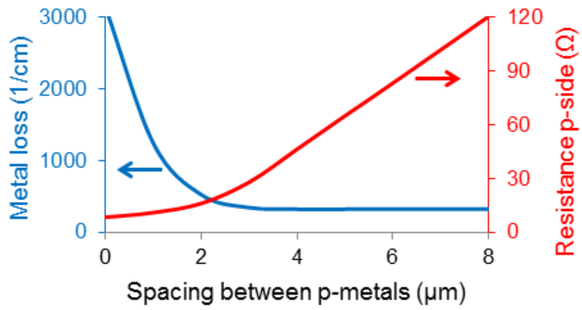

Fig. 3: Trade-off between metal loss and resistance.

spacing to be around 7 μm, which will result in a high resistance of 100 Ω. With a metal spacing of 3 μm which can be made with a p-side process, the resistance can be reduced below 30 Ω.

After processing on the p-side, planarization with BCB is required for the subsequent bonding process. In order to accurately control the BCB thickness and have a good thermal contact, an etch-back is usually performed. However, the etch-back on completely cured (at 280 ºC) BCB creates uniformity issues and affects the bonding. To mitigate this, a new technique involving partial cure at 180 ºC, followed by etch-back and complete cure, is developed. Experiments show good uniformity and reproducibility. The remaining processes are performed from n-side after the bonding.

N-type contact technology: Another contribution to the RC constant limitation comes from the n-type contact on the top of the PD. The specific contact resistance has to be optimized below 1×10^{-6} Ω cm^2 for a total resistance of the PD of less than 50 Ω. In our tests, Ni/Ge/Au based n-type contact shows a low contact resistance of 4×10^{-7} Ω cm^2 after 15 s annealing at 400 ºC. However, Au spiking during high temperature process is a well-known problem of this type of contact. This is critical for thin membrane devices: the Au spiking into the active layers can cause high optical loss and large leakage current. Therefore a new contact technology is developed by controlling the Au addition to the Ni/Ge contact. A circular transfer length method (CTLM) is used to measure the specific contact resistances of samples with different amount of Au participating in the annealing. The samples without Au addition give higher specific contact resistances (above 2×10^{-6} Ω cm^2). This is consistent with previous research showing the contribution of Au to the ohmic behavior.[3] Interestingly, by adding a very small amount of Au (20 nm deposition) the resistance drops to 7×10^{-7} Ω cm^2. As can be seen from Fig. 4a, this limited addition of Au leads to a very sharp and uniform interface between metal and InP. A thickening layer of Ti/Au can be deposited after the annealing without affecting the interface. Compared to the rough interface (over 100 nm Au penetration, Fig. 4b) made by the conventional contact (with 250 nm Au), this new technique provides a way to control the spiking while maintaining a low resistance.

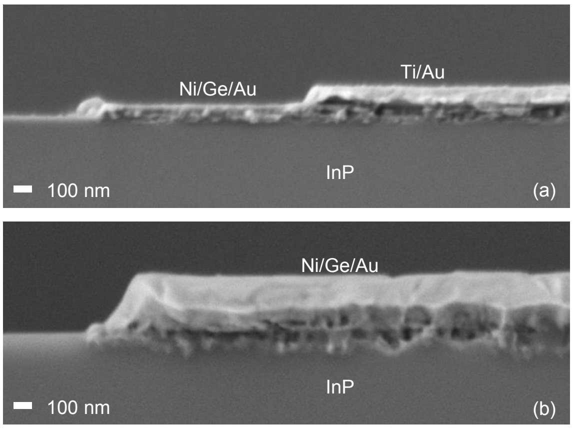

Fig. 4: SEM pictures of cleaved cross-sections.

Conclusion: A high-speed UTC-PD is designed in the IMOS platform. The carrier transit time is minimized below 2.5 ps by using the UTC structure. The strong absorption in the membrane leads to a compact size and a capacitance below 10 fF. A new double-side process technology and an optimized n-type contact scheme are developed to reduce the total resistance below 50 Ω. A 3 dB bandwidth beyond 100 GHz can be reached based on these values. Realization of the device is underway.

References

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