CMOS Photonic Integrated Circuits and Systems

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Abstract: Integrated photonic-electronic components and subsystems are designed and demonstrated for microprocessor-to-memory interconnection. Monolithically integrated receivers and transmitters are demonstrated in both zero-change silicon-on-insulator CMOS as well as custom bulk CMOS processes.

CMOS photonics applications include medium reach links for data center backhaul, short reach links for optical backplanes, optical implementations of peripheral hardware bus (PCI-type), memory-to-core links, and core-to-core links. Here we consider one particular application – memory-to-core links required for the continued scaling of multicore microprocessors.

Here, I review the progress made towards building systems utilizing CMOS electronics and photonics fabricated simultaneously within a state-of-the-art CMOS manufacturing flow. I will focus primarily on the recent results of devices and systems resulting from an on-going collaboration between my group (the Physical Optics and Electronics Gorup) at MIT, Vladimir Stojanovic's Group at UC Berkeley, and Milos Popovic's Group at the University of Colorado at Boulder. Recently, we have successfully demonstrated monolithic integrated electronic-photonic integration of transmitters (modulators and drive electronics) and receivers (photodetectors and circuits) in both foundry silicon-on-insulator processes as well as custom bulk CMOS processes.

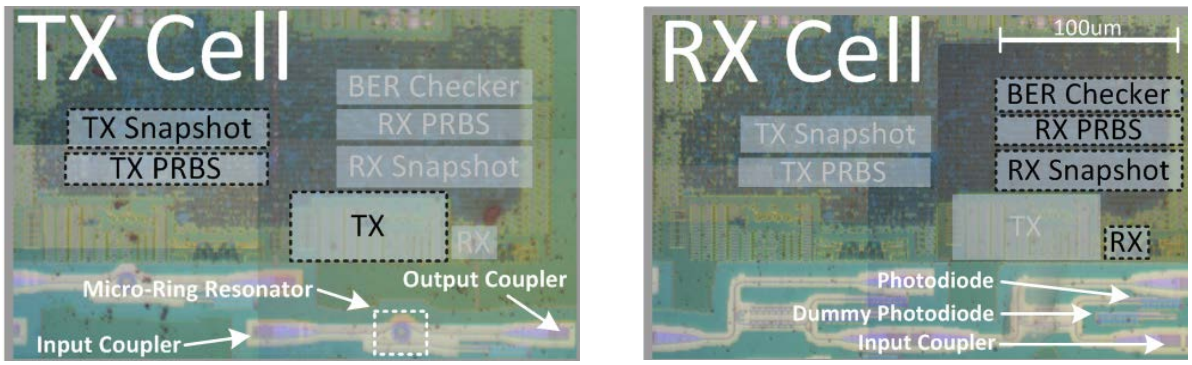

Fig. 1 a) Monolithically integrated transmitter in 45nm SOI with digital back-end. The micro-ring resonator uses interleaved p-n junctions to achieve efficient tuning in depletion mode. B) Monolithically integrated receiver in 45nm SOI utilizing SiGe photodetector.

Zero-change silicon-on-insulator CMOS photonics has been demonstrated using the IBM 45nm SOI platform. This unmodified platform is used for a wide range of products from supercomputers to servers to gaming consoles. Our team has demonstrated high-performance resonant modulators utilizing the crystalline (body) silicon as a waveguide layer. Optimized devices demonstrate 5 Gbps data transmission with an extinction ratio of 8 dB an insertion loss of 1.5 dB [1]. Interleaved p-n junctions are operated in depletion by virtue of electrical contacts distributed within the inner circumference of the ring-resonant modulator. The low capacitance of this structure results in a low-energy per bit of < 5fJ/bit for the intrinsic modualtor. When driven with an CMOS driver, the total energy consumption for the transmitter block is 20 fJ/bit at 2 Gbps [2]. To the best of our knowledge, this is the lowest energy consumption for an integrated transmitter. The receiver in this chip is realized by

exploiting interband absorption in the SiGe p-doped strain layers. These are the first waveguide infrared photodetecotrs implemented in a zero-change CMOS process. The 10% quantum efficiency detectors are coupled to an on-chip transimpedance amplifier and digital sense amplifier. The total power dissipation for the receiver is 220 fJ/bit at 2 Gbps [2].

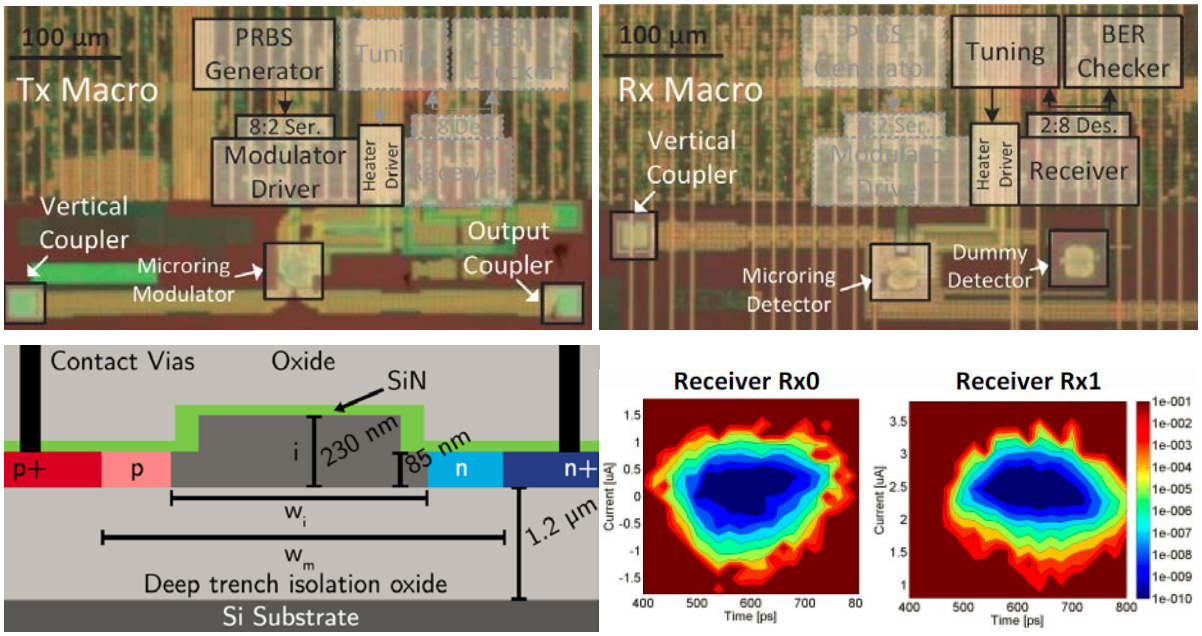

Fig. 2 a) Monolithically integrated transmitter in Bulk CMOS with digital back-end. A simple ridge waveguide microring resonator is used for transmission. b) Monolithically integrated 1280nm receiver in using defect state absorption in polysilicon based microring resonator. c) The cross-section of the polysilicon detector showing the layers for the polysilicon ridge waveguide and deep trench oxide. d) Link data transmission at 5 Gbps with direct fiber connection from chip-to-chip. The BER for the dual-data rate receivers is below 1e-10 for 5 Gbps operation.

Because of pricing sensitivity in a very competitive market, DRAM is fabricated only in bulk CMOS processes. Hence, the transmitter and receiver must be fabricated from a polysilicon layer that is deposited on a deep trench oxide. A complete photonic link has been demonstrated at 5 Gbps that transfers digital information from one Bulk CMOS Photonics chip to another [3]. A single-polysilicon deposition and lithography mask were used to simultaneously define the transistor gate, the low-loss waveguides, the depletion modulators, and the photodetectors [4]. The process was finely tuned to adjust the density of localized electronic states associated with the grain-boundaries in polysilicon. A low-defect state density was utilized for the waveguide and modulator layers. This defect state density could be tuned to be higher for the all-silicon photodetectors. The resulting microring resonant detectors exhibit a 20% quantum efficiency with 9.7 GHz bandwidth over a wide range of wavelengths [5]. For link tests, 1280nm laser was coupled into the transmitter chip, modulated, and then coupled into a receiver chip several meters away.

1. M. Wade, et al. Optical Fiber Conference, 2014.

2. M. Georgas, et al. VLSI Symposium, 2014.

3. C. Sun, et al. VLSI Symposium, 2014

4. R. Meade, et al. VLSI Symposium, 2014

5. K. K., Mehta, et al. Optics Letters, 2014