Design and Fabrication Technology for a Twin-Guide SOA Concept on InP membranes

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Abstract: In this contribution we present a novel concept of a twin-guide SOA design based on the "InP membrane on Si" (IMOS) platform. As a fundamental device, this SOA design can be used for lasers with current injection and photodetectors under reverse bias in the IMOS platform. The fabrication scheme is presented in detail and the current fabrication progress will be shown.

Introduction: The InP membrane on Si (IMOS) technology [1] is a novel candidate for resolving the on-chip data communication bottleneck by adding an additional III-V photonic layer on top of electronic chips. The major advantage of this platform is the possibility to integrate passive (waveguides, filters) and active components (lasers, photodetectors) in a single membrane.

A variety of passive IMOS components have been demonstrated with good performance in past few years. However, as a fundamental element to be used in active membrane devices, the optical amplifier (SOA) is not yet demonstrated.

In this contribution, we present a novel design of a twin-guide SOA structure on the IMOS platform. The proposed SOA design can be used both in lasers and photodetectors with good predicted performance. The fabrication scheme is presented in detail and the current fabrication progress will be shown.

SOA Design: The SOA design is based on the so-called twin-guide approach. It consists of two vertically stacked waveguiding layers; for the active and the passive functions respectively. The complete SOA structure including material and layerstack information is depicted in Figure 1(a). After being bonded to a Si carrier wafer using DVS-BCB as the bonding material, the SOA layerstack consists of (from low to high): a 300 nm thick InP passive waveguiding layer; 100 nm thick n-contact layers formed by a n+-doped quaternary layer (Q1.25) and an n-doped InP layer; a bulk active region formed by 250 nm thick nominally undoped
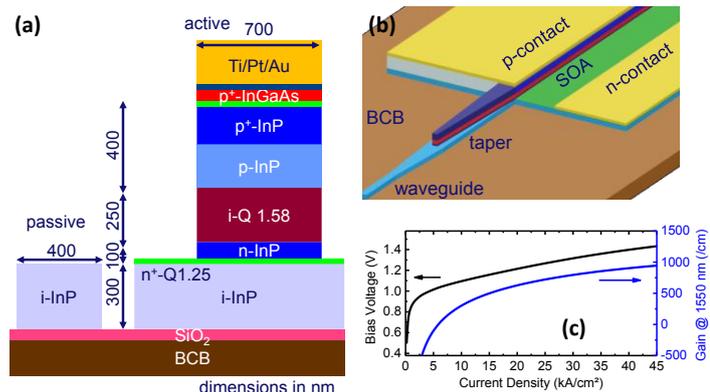

Fig. 1 (a) The schematic picture of the proposed SOA structure. (b) The 3D schematic picture of the taper structure between SOA and waveguide. (c) Simulated I-V characteristics and material gain of the active layer as a function of current density.

Q1.58; a p-doped InP cladding layer; a p-contact region formed by quaternary spacer layers and highly p+-doped InGaAs. To define the amplifier, 700 nm wide ridges are defined by means of dry etching until the n-doped contact layer. The designed SOA width ensures a fundamental transverse electric (TE) mode in the active region with a high confinement factor (0.55) and an affordable absorption loss (~50 cm^{-1}). The p-side of the SOA will be contacted using a Ti/Pt/Au metallization on top of the ridge, while the n-side will be contacted with Ni/Ge/Au pads parallel to the ridge with a few micrometer separation. In the passive regions, all layers except the 300 nm InP waveguiding layer are removed by a combination of dry and wet etching. The transition of the optical power between the SOA and the passive waveguide is accomplished by a taper structure, as shown in Fig. 1 (b). The 3D-FDTD simulations show a taper length of 10 μm is sufficient to transfer 95% of the light between the SOA and waveguide.

To estimate the material gain in the active layer, electrical simulations using a self-consistent 1D Poisson-solver (nextnano++) are performed. The corresponding I-V characteristics of the diode

(including the series resistance of the contacts) is plotted in Fig. 1(c) as black line. The material gain is then calculated from the charge carrier density as a function of the current density [2] up to 45 kA/cm . Auger recombination, radiative and surface recombination are all considered in the model using typical values from literatures. The material gain of the active layer at 1550 nm wavelength is plotted in Fig. 1(c) as a blue line. The current density to compensate the loss in the amplifier is estimated to be 6.8 kA/cm at a voltage of 1.05V.

The main advantage of this design is that all the fabrication steps will be done after bonding. This avoids problems of bonding quality and increases yield. The fabrication process to realize the SOA design is described in the next section.

Fabrication: The key fabrication steps for the twin-guide SOA structures as well as the passive waveguides are depicted in Fig. 2. The fabrication starts with the flip-chip BCB bonding of the III-V layerstack onto a SiO₂/Si carrier wafer, followed by removing the InP substrate and an InGaAs sacrificial layer wet-chemically. After bonding, the SOA pattern is defined using electron beam lithography (EBL) with C_{60}/ZEP resist and a SiN_x hard mask [3]. The pattern is finally transferred with dry etching to the III-V layerstack. The etching is stopped when the n-doped InP layer is reached (Fig. 2a)). The region for making n-type metal contact is defined
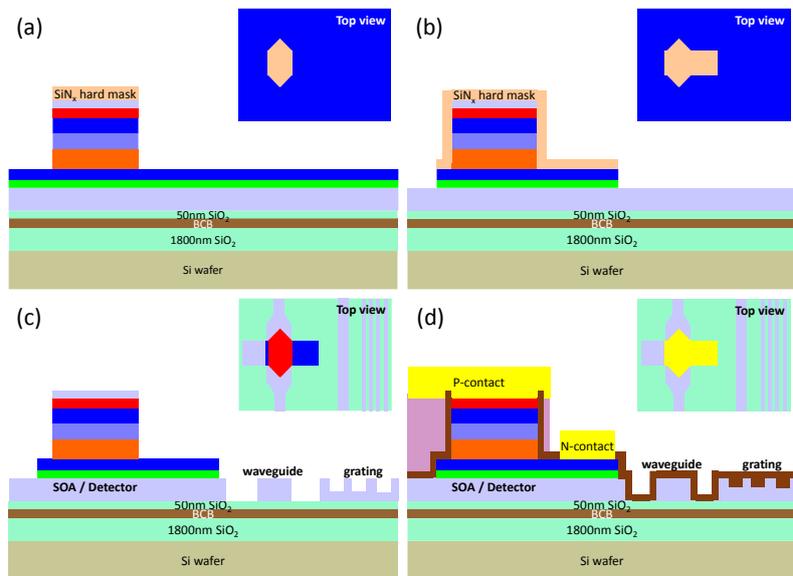

Fig. 2 (a) The first EBL step to define the SOA structure on the bonded sample. b) The second EBL step to define the n-contact region. c) The third and fourth EBL step to print the passive waveguides and fiber-grating couplers. d) The lift-off step to create p and n metal contacts.
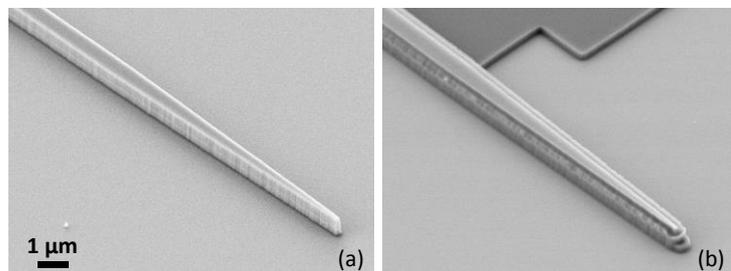
with a second EBL. The SiN_x will protect the regions where n-InP and n-Q1.25 material are preserved for making the n-contacts. The n-type material at all the other regions will be removed wet-chemically (Fig. 2(b)). Two more EBLs will be performed to realize passive waveguides and fiber-grating couplers with etch depths of 300nm and 120nm, respectively, as shown in Fig. 2(c). During the final metallization step, the entire sample is covered with a 50-nm thin SiN_x layer for electrical isolation and planarized with polyimide. Finally two lift-off processes using optical lithography are performed to create the p- and n-metal contacts, as shown in Fig. 2(d). It is worth to mention that all the processings (including dry and wet etching, optical lithography, surface treatment etc.) are based on mature technologies from the COBRA standard multi-project wafer runs [4], in order to ensure the reliability of the entire fabrication.

Currently a test fabrication run of the SOA structure using the described layerstack is well underway. The SEM pictures taken in between some fabrication steps are presented in Fig. 3. First results make us confident that we can reliably fabricate laser devices in the near future.

Fig. 3 The SEM picture of the taper structure of the SOA (a) after 1st EBL and dry etching to form the SOA ridge, (b) after 2nd EBL and wet etching of the n-contact material.

References

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