# Si-Wire based 8 × 8 strictly-Non-Blocking PILOSS Switch

**Keijiro Suzuki,** **Ken Tanizawa, Takashi Matsukawa, Guangwei Cong, Sang-Hun Kim,**
**Satoshi Suda, Morifumi Ohno, Tadashi Chiba, Hirofumi Tadokoro, Masashi Yanagihara,**
**Yasushi Igarashi, Meishoku Masahara, Shu Namiki, and Hitoshi Kawashima**

*National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan*
*k.suzuki@aist.go.jp, ken.tanizawa@aist.go.jp, t-matsu@aist.go.jp, gw-cong@aist.go.jp,*
*sanghun-kim@aist.go.jp, s-suda@aist.go.jp, morifumi-ohno@aist.go.jp, tadashi-chiba@aist.go.jp,*
*h-tadokoro@aist.go.jp, masashi-yanagihara@aist.go.jp, yasushi-igarashi@aist.go.jp, m.masahara@aist.go.jp,*
*shu.namiki@aist.go.jp, kawashima-h@aist.go.jp*

**Abstract:** We present a Si-wire waveguide based 8×8 path-independent insertion-loss (PILOSS) switch, which has a record-small footprint of $3.5 \times 2.4$ mm$^2$. The PILOSS switch includes 64 thermooptic Mach-Zehnder switches and 49 intersections. These switches and intersections employ directional couplers, which enable to comprise a low loss PILOSS switch. We demonstrate successful switching of digital-coherent 43-Gbps QPSK signal by the PILOSS switch.

## 1. Introduction

There is a continuing demand for strictly non-blocking high-port-count $N \times N$ optical switches in an integrated form [1, 2]. A standard $N \times N$ switch topology is a path-independent insertion loss (PILOSS) topology [3], in which light passes through $N$ element switches and $N-1$ intersections for all the $N^2$ ways. The number of ON (the switch with electric power applied is in ON state) elements is $N$ in the PILOSS topology. Another option is a "switch-and-select" topology, in which the switch is composed of $1 \times N$ switch units arrays [4-6]. The number of ON switch elements depends on a path setting, and the average number of ON elements is proportional to $(\log_2 N)$ $N$. Comparing the two topologies, the PILOSS switch is more energy efficient due to less ON switch elements. For this reason, we believe that the PILOSS remains prospective for long-term scalability towards larger $N$.

In this paper, we report the implementation of an 8×8 PILOSS switch using Si-wire waveguides. The PILOSS switch has record-small footprint of $2.4 \times 3.5$ mm$^2$. Crosstalk of the PILOSS switch is as low as $-23.1$ dB, comparable to the switch based on the thick ($\sim 1.5$ μm) Si-rib waveguides [7]. For circuit switch applications, 43-Gbps digital-coherent QPSK signals switching is also demonstrated.

## 2. Results and discussion

The $8 \times 8$ PILOSS switch chip fabricated by use of *e*-beam lithography and CMOS-compatible process are shown in Fig.1(a). The PILOSS switch includes 64 Mach-Zehnder (MZ) switches and 49 intersections. A Si-wire waveguide dimension is $430 \times 220$ nm$^2$, buried by SiO$_2$ over cladding. The MZ switch is composed of directional couplers and thermooptic phase-shifters with TiN heaters. A footprint of the PILOSS switch is $3.5 \times 2.4$ mm$^2$, which is 1/550 as small as that of the silica PLC switch [3], 1/4 as small as that of the thick Si-rib waveguide based switch [7]. The measured insertion losses at a wavelength of 1.55 μm are shown in Fig. 1(b). The average on-chip loss is $6.5 \pm 1.0$ dB, where the on-chip loss is defined as the loss without the coupling loss. This small loss variation clearly warrants the merit of the PILOSS topology. Figure 1(c) plots the crosstalk for all switch states ($8! = 40,320$) that was estimated from the results of the loss measurement [8]. The crosstalk is lower than $-18.3$ dB, and its median is $-23.1$ dB. The crosstalk is limited by the switch-to-switch variation of the minimum-crosstalk wavelength, which is estimated to be $\sim 5$ nm.

We evaluated the switching characteristics of a digital-coherent 43-Gbps QPSK signal between two switch states. Figure 2 shows the measured constellation diagrams of each output port for the state 1 (input-output connections are 1-8, 2-7, 3-6, 4-5, 5-4, 6-3, 7-2, and 8-1) and 2 (1-1, 2-6, 3-4, 5-2, 6-5, 7-3, and 8-8). It is found that there are clearly separated symbols and not any degradation at both switch states compared to the back-to-back result. The measured error vector magnitude is approximately 13.4%, corresponding to a BER of less-than $1 \times 10^{-12}$.

These results demonstrate that the Si-wire based PILOSS switch can be a good candidate for the high-port-count strictly-non-blocking $N \times N$ switch in the integrated form. The wavelength and polarization dependence of the PILOSS switch are yet challenges to be solved [9].
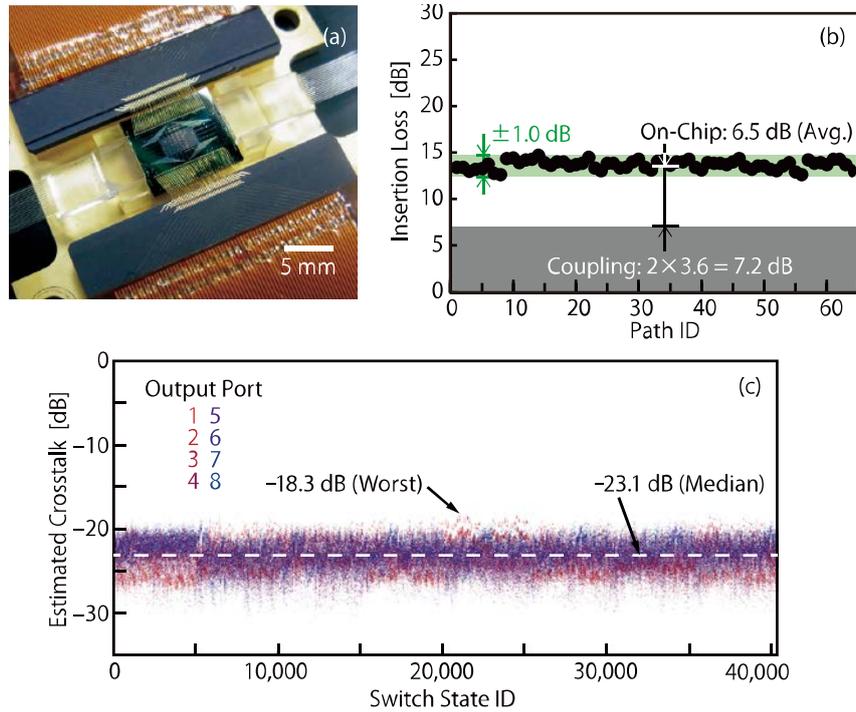


Fig. 1: (a) Fabricated 8×8 PILOSS switch on ceramic mount. (b) Fiber-to-fiber insertion loss of $8^2$ =64 paths. (c) Estimated crosstalk at eight output ports for all possible switch state (8! = 40,320).
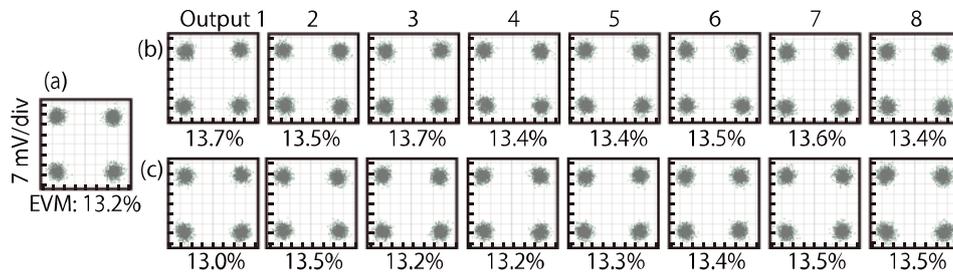


Fig. 2: Measured constellation diagrams. OSNR = 20 dB. (a) Back to back. (b) State A (input-output: 1-8, 2-7, 3-6, 4-5, 5-4, 6-3, 7-2, and 8-1). (c) State B (1-1, 2-6, 3-4, 5-2, 6-5, 7-3, and 8-8). EVM: Error Vector Magnitude.

## Acknowledgement

## References

1. S. Namiki, et al., IEEE J. Sel. Top. Quantum Electron. **17**, pp.446-457 (2011).
2. K. Ishii, et al., Proc. SPIE **8646**, pp.86460A (2013).
3. T. Goh, et al., J. Lightwave Technol. **17**, pp.1192-1199 (1999).
4. L. Chen, et al., Opt. Express **20**, pp.18977-18985 (2012).
5. M.-J. Kwack, et al., Opt. Express **20**, pp.28734-28741 (2012).
6. S. Nakamura, et al., OFC/NFOEC'12, OTu2I.3 (2012).
7. S. Nakamura, et al., Proc. OFC'11, OTuM2 (2011).
8. K. Suzuki, et al., Opt. Express **22**, pp.3887-3894 (2014).
9. S.-H. Kim, et al., ECOC, We.4.B.5 (2013).