Technology achievements for silicon photonic devices

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***Abstract*— Silicon Photonic high performance generic building blocks will be reviewed such as few mW sources by III-V/Si heterogeneous integration, 40G Si modulators and Ge detectors for interchip communications.**

Keyword: silicon photonics, hybrid lasers, silicon modulator, germanium photodetector.

I. INTRODUCTION

In the last years, submicron silicon photonics have generated an increasing interest in the recent years, mainly for optical telecommunications or for optical interconnects in microelectronic circuits. The rationale of silicon photonics is the reduction of the cost and energy of communications systems through the integration of photonic components and an electronic integrated circuit (IC) on a common chip (telecommunications applications), or the enhancement of IC performance with the introduction of optics inside a high performance chip (core to core communications), or low cost sensors. By co-integrating optics and electronics on the same chip, high- functionality, high-performance and highly integrated devices can be fabricated with a well-mastered microelectronics fabrication process. In addition, advances in CMOS photonics will move the emphasis from device component to architecture. The FP7 HELIOS project aims to combine a photonic layer with a CMOS circuit by using microelectronics fabrication processes. It will make CMOS photonics accessible to a broad circle of users in a foundry-like, fabless way. The objectives of the project are manifold and one is the development of high performance generic building blocks for a broad range of applications: WDM sources by III-V/Si heterogeneous integration, fast modulators and detectors, passive circuits and packaging.

2. Hybrid InP directly bonded on Si sources

The heterogeneous integration of III-V materials by bonding consists in the transfer an III-V heterostructure from its original growth substrate to a silica surface. The III-V components are then fabricated on 200mm SOI processed wafer using wafer-scale processing. This technique allows a high density of integration, collective processing and the use of high-quality III-V layers. Light can be directly coupled into a silicon waveguide underneath the III-V epitaxy. Most of the laser functions can be moved into the silicon part by designing the III-V layer only as a gain material while the cavity lies in the silicon region. The III-V heterostructure (InP based stack) are placed only at specific location by die-to-wafer bonding. The strong point is that it reduces the cost of the integration process since expensive III-V stacks can be bonded only where they are needed (fig 1).

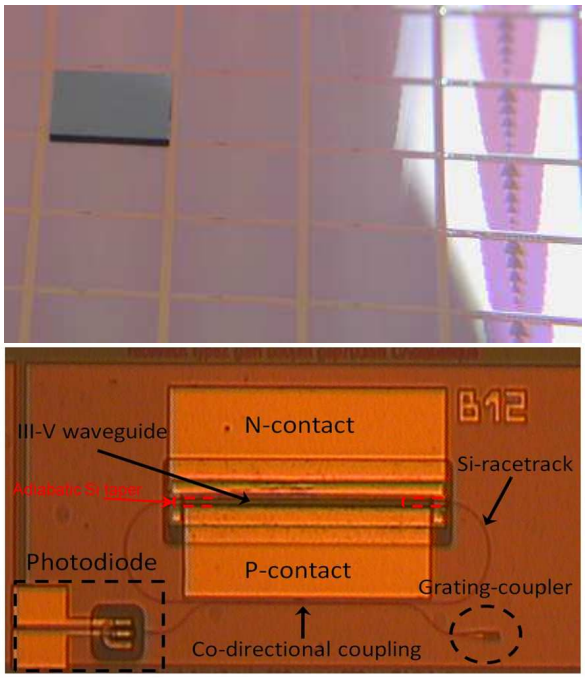

Figure 1: InP die on silicon photonics circuit with SiO_2 molecular bonding and view of fabricated lasers on Si

After molecular bonding, mechanical grinding and InP chemical etching are performed in order to leave the thin heterostructure on the waveguide layer with a controlled SiO2 separation layer. Decontamination steps of the rear side of the wafers are required before the introduction of the wafers in a microlectronics fab at the back-end level. With DeepUV lithography, fine patterns can be defined with high alignment with the waveguide layer. Then etching of InP in 200mm format is performed using reactive ion etching (RIE) with CH4/H2 gases as the thin thickness of the heterostructure requires low etching speed. The defined InP structures for SOA or laser are then cladded with a thick silica before openings for electrodes formation [1].

Despite the lack of engineering of the current flow, the ring laser operates under continuous mode. Derived from the L-I characteristics, the laser threshold is 30 mA with a maximum output power of 6 mW at 15 °C giving about 3mW in the output fiber. For monitoring, a photodiode was defined with

the III-V stack. The dark current is 1nA and without optimization, the sensitivity is 0.3 A/W [2].

3. Si modulators

Modulation in silicon is usually obtained by free carrier concentration variation. Carrier depletion is a high speed effect that has been widely used to achieve fast modulators [3]. Thick modulators (400nm) have been also fabricated based on carrier depletion in a PIPIN diode in the Helios project, demonstrating large 40 Gbit/s-extinction ratio simultaneously with low optical loss. A schematic view of the device cross section is shown in Fig. 2. The silicon rib waveguide width is 420 nm, the rib height is 390 nm and the etching depth is 290 nm, leading to quasi-TE and quasi-TM single mode propagations at a wavelength of 1.55 µm [4].

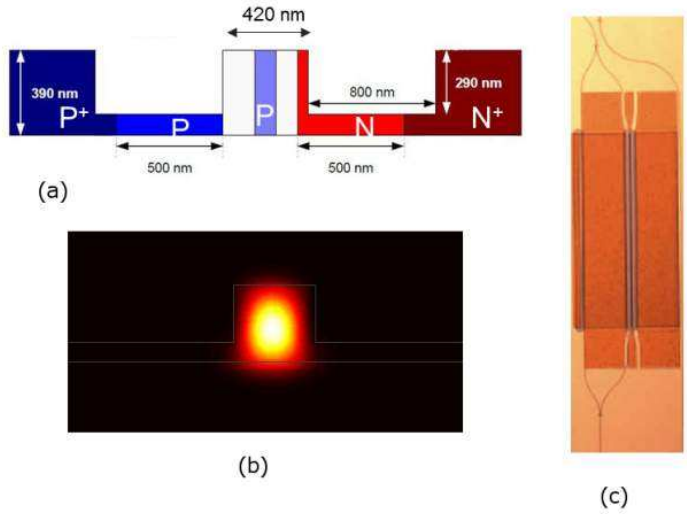

Figure 2: (a) Schematic view of lateral PIPIN phase shifter; (b) Optical mode profile at 1.55 µm; (c) Optical microscope view of the MZI modulator

Compared to a regular PIN diode, a P-doped slit with a nominal doping concentration of 3.10^{17} cm-3 is inserted in the intrinsic region of the lateral PIN diode and acts as a source of holes. Optical loss is then reduced because a large part of the waveguide is not intentionally doped, and the metallic contact regions are far from the light propagation area. At equilibrium, holes are confined in the p-doped slit centered in the rib. When a reverse bias is applied to the diode, holes are swept out of the active region. The optical modulator is fabricated on a 200mm SOI wafer with a 2 µm BOX and a 400 nm silicon film with microelectronic tools such as Deep-UV optical lithography and RIE. A self-alignment technique was used to guarantee the Boron implantation in the middle of the waveguide, to align the left P and right N doped region at the border of the waveguide. This guarantees the repeatability of the results from die to die on a wafer.

A silicon optical modulator based on a reverse biased pipin diode embedded in a Mach-Zehnder interferometer working at 40 Gbit/s was demonstrated. Two phase shifter lengths were presented, one 0.95 mm long with an ER of 3.2 dB, and an optical loss of 4.5 dB, and one 4.7 mm long with an ER of 6.2 dB, and an optical loss of 6 dB. Further improvements can be considered, including the increase of the doping level in the active region and a push-pull operation to increase the ER.

4. Ge photodetectors

High speed and high responsivity germanium photodetectors have been fabricated in the Helios project and exhibited a zero-bias 40Gbit/s pin Ge photodiode integrated at the end of a Si waveguide using the butt coupling approach [5]. A 10µm long silicon recess was etched at the end of the waveguide (220nm thick, 500nm wide) down to a thin silicon layer of about 50nm. Ge was selectively grown by RP-CVD in the Si cavity. A thick silica layer which can block the implantation, was deposited and a self-aligning process was used to perfectly to define the gap between n-type and p-type doped regions of the Ge PD, that were implanted with phosphorous and boron ions, respectively. Changing the width of the gap modify the transit time and thus the bandwidth. Electrodes were then defined withTi/TiN/AlCu metal stack deposition and etching. The photodetectors were connected to a demux composed of a 2D surface grating coupler and two 16 channels AWG (Fig 3) to define a 16 channels receiver.

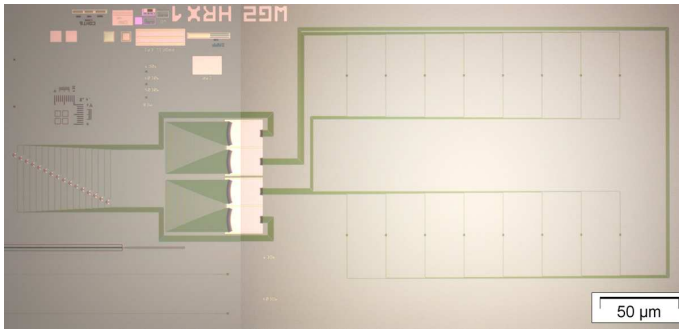

Fig. 3: Top-view Optical Microscopy of the 16 channel receiver with 2D couplers (left) and Ge PD before metallization (right).

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