

Integration and Packaging of Optoelectronic and Silicon Photonic Chips on a μm -scale SOI Platform

Timo Aalto, Mikko Harjanne, Markku Kapulainen and Sami Ylinen

VTT, Espoo, Finland
firstname.lastname@vtt.fi

Abstract—An overview of an integration platform with 1–10 μm thick silicon-on-insulator waveguides is given. It is suitable for the integration and packaging of optoelectronic and silicon photonic (nm-scale) chips. The platform can also contain many passive functions, such as spot-size converters, couplers, wavelength (de)multiplexers/filters and polarization splitters. The footprint of the platform is minimized by using multi-step patterning to realize e.g. mirrors and short MMI couplers.

Keywords: Silicon-on-insulator; SOI; integration platform; silicon photonics; optoelectronics; hybrid integration; packaging

I. INTRODUCTION

Development of single mode (SM) silicon-on-insulator (SOI) waveguides started in early 1990's and has also been carried out at VTT since 1997. With deep UV lithography the dimensions of SOI waveguides have been reduced from micrometers to <100 nm, and advanced photonic circuits have been realized on nm-scale SOI platforms [1]. At the same time also III-V compound semiconductor optoelectronics has evolved significantly and is now widely used in numerous application areas, such as optical communication, consumer electronics, lighting and sensing. Heterogeneous integration [1–3] has also been developed to combine the complementary benefits of III-V optoelectronics and Si photonics. Increasing the level of integration aims to improve device performance and to reduce cost, power consumption and footprint. To exploit the new technologies in a wide range of applications, and to tackle the thermal and I/O coupling challenges also new packaging methods must be developed [1–3].

This paper first presents a generic platform on 1–10 μm thick SOI that is used to hybrid integrate optoelectronic chips on a passive photonic SOI circuit. A new packaging concept that can be used to integrate also Si (nano)photonic chips, to provide hermetic sealing and to couple light with large fiber arrays is then proposed.

II. PHOTONIC CIRCUITS ON THE SOI PLATFORM

Silicon-on-insulator wafers and chips are here used as a generic integration platform. In general the device layer thickness can be anything from <1 to >10 μm , but here we mainly concentrate on 4 and 10 μm SOI layers where most of the devices reported here have been built. Single mode rib waveguides can be easily realised by dry etching $\sim 50\%$ of the SOI layer thickness. With an additional $\sim 50\%$ etch step it is

possible to gradually convert the rib waveguide into a multi mode strip waveguide without exciting the higher order modes. The same etch step can be used to locally reduce the waveguide thickness, e.g. to achieve better coupling to other optical chips. This multi-step patterning concept is also used to realize and improve many other waveguide components. [1]

The minimum bending radii of rib waveguides are strongly dependent on the SOI thickness, but photonic circuits with small footprint can be realized even on 10 μm SOI using mirrors to turn light horizontally. Also up-reflecting mirrors have been demonstrated to enable optical coupling from/to surface-active optoelectronic components, as well as for wafer-level testing. These wet-etched and metal-coated mirrors are placed behind antireflection (AR) coated waveguide facets. Such facets can also be placed at the edges of the SOI chips to enable reflection-free I/O coupling to e.g. optical fibers.

Passive couplers (1x2, 2x2 etc.) are the basic building blocks of waveguide circuits and they have been demonstrated in various directional, multimode interference (MMI) and adiabatic coupler configurations on SOI. Through-etched MMI 2x2 couplers can be made as short as 285 μm in 4 μm SOI, while adiabatic couplers can have >20 dB extinction ratio (ER) and <1 dB insertion loss at >100 nm bandwidth. Couplers have also been cascaded into Mach-Zehnder interferometers (MZIs) to realize thermo-optic (TO) switches (up to 333 kb/s [5]), wavelength multiplexers and polarization splitters. Also arrayed waveguide gratings (AWGs) have been realized on SOI. By using back-reflecting mirrors and a single star coupler it is possible to realise compact AWGs even on 10 μm SOI. Some SOI waveguide components are illustrated in Fig. 1 and some measured component characteristics are listed in Table I.

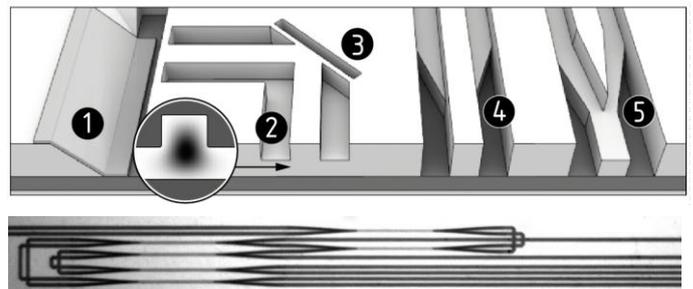


Figure 1. Illustration of some key optical components: 1) Up-reflecting mirror, 2) Single mode rib waveguide, 3) Horizontal mirror, 4) Rib-strip converter, and 5) Vertical taper (above). Microscope image of a compact four-channel MUX built using asymmetric MZIs and horizontal mirrors (below).

TABLE I. MEASURED PERFORMANCE EXAMPLES ON SOI

Component (SOI thickness)	Performance	Property
SOI rib waveguide (4/10 μm)	0.1 dB/cm	Propagation loss
Vertical taper (4 \rightarrow 2 μm) ^a	0.2 dB	Insertion loss
Rib-strip converter (4/10 μm)	0.05 dB	Insertion loss
Horizontal mirror (4 μm) ^a	0.3 dB/90°	Insertion loss
2x2 coupler (4 μm) ^a	0.3 dB	Insertion loss
TO switching/tuning (4/10 μm)	<1 μs	Response time
Polarisation splitter (4 μm) ^a	>10 dB	Extinction ratio
AWG (4 μm) ^a	2–6 dB	Insertion loss
(depending on number of channels)	20–30 dB	Extinction ratio

a. Similar values measured/expected for other SOI thicknesses in 4–10 μm range

III. HYBRID INTEGRATION ON THE SOI PLATFORM

There are three main methods to bond optoelectronic chips on the SOI waveguide platform, or on Si in general, namely soldering (e.g. with AuSn), thermo compression (TC) and adhesive bonding. In this paper we concentrate on Au-Au TC bonding and adhesive bonding. Some examples of optoelectronic chips bonded on SOI are illustrated in Fig. 2.

Thermo compression with $\sim 0.5 \mu\text{m}$ thick Au contact pads has been used to bond laser diodes, mode-locked lasers (MLLs), comb lasers and semiconductor optical amplifiers (SOAs) on 4 μm SOI and Si platforms. By accurately measuring the depth of the flip-chip mounts on SOI and by fine tuning the thickness of the deposited dielectric and metal films the vertical alignment between the optical axes of the SOI waveguides and the optoelectronic chips can be controlled with $\pm 100 \text{ nm}$ accuracy. The horizontal alignment accuracy is typically $\pm 1 \mu\text{m}$, but in some cases it can be as good as $\pm 500 \text{ nm}$. No performance degradation has been observed in the TC-bonded chips. An example of the measured performance of the optoelectronic assemblies is $>10 \text{ dB}$ net gain (incl. coupling losses) per SOA in hybrid integrated SOA bars that contain 11 SOAs per chip.

Single photodiodes and 4-ch photodiode arrays have been integrated on SOI using both TC and adhesive bonding. Top-illuminated photodiodes with integrated polymer prisms where TC bonded on SOI so that light from AR-coated SOI waveguide facets was reflected inside the prisms towards the flip-chip bonded photodiodes [6]. These single photodiodes were also able to collect light from 10 SOI waveguides that formed a star-coupler in front of the polymer prism. The inter-waveguide non-uniformity of the responsivity was $<0.05 \text{ A/W}$, while the absolute responsivity of $>0.7 \text{ A/W}$ was almost as high as in the discrete chips. And finally, back-illuminated photodiodes were glued on top of up-reflecting mirrors fabricated on SOI.

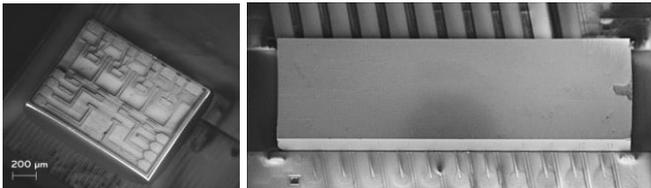


Figure 2. Active devices integrated on the SOI platform: Four-channel back-illuminated PD array (left) and 11-channel SOA array (right).

IV. SOI-BASED PACKAGING

Packaging method for an optoelectronic assembly should be selected based on the application-specific needs for mechanical protection, temperature control, electrical and optical I/O coupling, hermetic sealing etc. Conventional concepts use metals, ceramics and polymers as packaging materials [1–3], and these can also be used with the SOI platforms described here. However, in this paper we propose a new packaging concept (see Fig. 3) that combines chip-to-wafer bonding, through-silicon vias (TSVs), wafer-level sealing with a Si cap and passive fiber alignment. Most of these building blocks have already been demonstrated and in future they will be combined to realize advanced optoelectronic modules that provide significant cost and size reductions, improved thermal management and low I/O coupling losses. This Si/SOI-based packaging concept can be used for both optoelectronic and Si (nano)photonic chips. By default the platform will be based on 10 μm SOI equipped with vertical tapers and up-reflecting mirrors to achieve good coupling to standard SM fibers and to all hybrid-integrated devices, with wide bandwidth and low polarization dependency.

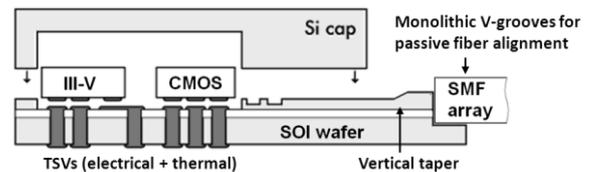


Figure 3. Simplified illustration of the proposed packaging concept.

ACKNOWLEDGMENT

The authors thank Ville Vilokkinen from Modulight Oy, Ludwig Mörl from Heinrich Hertz Institute, Mircea Guina from Tampere University of Technology, Vladimir Mikhrin from Innolume GmbH and Marcel Kroh from u2t Photonics AG for providing the optoelectronic chips for the hybrid integration experiments.

REFERENCES

- [1] C. Kopp et al., "Silicon photonic circuits: On-CMOS integration, fiber optical coupling, and packaging," *IEEE J. Sel. Top. Quantum. Electron.*, vol. 17, pp. 498–509, May/June 2011.
- [2] L. Zimmermann, G. Preve, T. Tekin, T. Rosin, and K. Landles, "Packaging and Assembly for Integrated Photonics—A Review of the ePIXpack Photonics Packaging Platform," *IEEE J. Sel. Top. Quantum. Electron.*, vol. 17, pp. 645–651, May/June 2011.
- [3] T. Tekin, "Review of packaging of optoelectronic, photonic, and MEMS components," *IEEE J. Sel. Top. Quantum. Electron.*, vol. 17, pp. 704–719, May/June 2011.
- [4] K. Solehmainen et al., "Development of multi-step processing in silicon-on-insulator for optical waveguide applications," *J. Opt. A: Pure Appl. Opt.*, vol. 8, pp. S455–S460, 2006.
- [5] M. Harjanne, M. Kapulainen, T. Aalto, and P. Heimala, "Sub- μs switching time in silicon-on-insulator Mach-Zehnder thermo-optic switch," *Photonics Technol. Lett.*, vol. 16, pp. 2039–2041, 2004.
- [6] L. Moerl et al., "Optical coupling of planar III-V pin photodiodes and SOI waveguides using an integrated BCB prism," *Proc. IPRM 2010* (Kagawa, Japan, 31 May - 4 June 2010), pp. 1–4, 2010.