Optical Interconnects to Chips

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Abstract— **This tutorial will introduce the requirements on reducing energy and increasing density in future interconnects beyond the capabilities of wires, and discuss resulting requirements on optical and optoelectronic devices and technologies for interconnects to chips.**

Keywords-optical interconnects; modulators; plasmonics

Power now dominates as a major constraint in information processing, and it will remain so for the foreseeable future and beyond. Already we cannot connect all the transistors and processors to one another or to memory or the outside world at the desired bandwidths without generating too much heat. This power dissipation not only constrains performance within the box; it also leads to economic and environmental limits [1]. In addition, topological and bandwidth density limitations of electrical wiring already limit longer interconnections, limitations that optics can readily remove.

Optics can in principle solve the energy problems of interconnects while also allowing higher interconnect densities, especially for longer off-chip distances [1,2]. The underlying physics is that optical interconnects only have to drive the optical transmitter devices and charge the photodetectors, not charge the capacitance of an electrical line to the signal voltage, a benefit of optics that ultimately comes from the quantum nature of light – in particular, the photoelectric effect.

The challenges with optics, however, are to come up with optoelectronic devices that themselves require low enough drive energies that they offer a practical benefit, and to generate technology that can be manufactured in large volumes at low cost. Electrical wires operate at energies of ~ 1 pJ/bit or higher for off-chip interconnects and ~ a few 100 fJ/bit to ~ 1 pJ/bit for global on-chip interconnects. To give sufficient energy benefit, therefore, total system energy of < 100 fJ/bit will be required for optical interconnects to chips, and this in turn means we will require optical output devices (lasers or modulators) that are efficient at ~ 10 fJ/bit transmitter energies, and optical receivers (photodetectors and associated circuitry) that can operate with < 1 fJ/bit of received energy. Large volume manufacture likely requires that we can exploit technologies such as silicon integrated circuit manufacture. We likely also require that the optoelectronics technology is very well integrated with electronics so that the capacitances between devices and electronic drive and receiver circuits can be kept low enough for good enough energy performance.

These energy numbers are aggressive targets for optoelectronic devices, though they are not unphysical. Various device technologies are now being explored as low-energy modulators that could be integrated with silicon manufacture in the growing field of silicon photonics, such as silicon-based modulators [3], for example. Quantum-confined Stark effect (QCSE) quantum well modulators are one possible transmitter approach that could scale to particularly low numbers, including sub-fJ operation in recent Ge devices on Si [4, 5]. Photodetectors with capacitances in the fF range are possible with tightly integrated approaches such as small Ge detectors on Si. Nanophotonic resonators and nanometallic antennas for confining light to very small subwavelength scales [6] might allow devices to operate into the aJ/bit range.

For interconnects it will also be important to make optical devices such as wavelength splitters very small. One important opportunity is to exploit nanophotonic structures for new generations of such components. For example, particularly small wavelength splitters might be possible with non-periodic superprism structures [7] or by innovative nanometallic approaches [8].

In summary, these and other approaches to novel optical and optoelectronic devices exploiting nanophotonics and quantum confinement are very promising for future applications such as optical interconnects, and such interconnects may be the key to enabling future information processing systems to continue to scale in performance.

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