PICs: A Commercial Future

Michael J. Wale
Oclaro Technology Ltd.
Caswell, Towcester, Northamptonshire, NN12 8EQ, UK
Mike.Wale@oclaro.com

***Abstract* — Photonic Integrated Circuit (PIC) technology offers attractive, cost-effective solutions for many applications. This paper reviews the present status of commercial exploitation and suggests new approaches to design and manufacture which could enhance availability and exploitation.**

Keywords - photonic integration, PIC, integrated optics

I. INTRODUCTION

Photonic integrated circuit (PIC) technology has now reached a high level of capability and is being exploited in important applications, particularly in telecommunications. By allowing many of the fundamental building blocks of photonic systems (optical amplifiers, lasers, modulators, couplers, waveguides, etc.) to be combined on a single chip, PICs can provide important benefits in terms of cost, size and manufacturability over solutions based on discrete elements. Such a versatile technology should have many applications across the industry. This paper examines the current status and suggests developments that could facilitate just such a market expansion.

II. CURRENT STATUS

PIC technology was originally developed in response to the needs of the telecommunications industry. In Europe, numerous collaborative R&D projects, supported by the EU, provided an impetus and support for these developments. In this paper, we shall focus particularly on PICs based on III-V semiconductor materials such as InP, which can support active functions (amplifiers, lasers) alongside modulation and passive elements such as wavelength multiplexers. InP-based PICs are now in volume production for several important applications in telecommunications, such as integrated transmitters and receivers for high-speed fibre optic links in the core of the network. Fig. 1 shows a wafer of integrated InP-based tunable laser-modulator devices [1,2] under test at Oclaro's wafer fab at Caswell, UK. These devices provide the photonic core of a tunable 10Gbit/s transceiver using the industry-standard 'XFP' format. Devices with similar functionality are presently being manufactured by at least two other companies in Europe and the USA. The demand for these and similar components is substantial and at an annual level of several hundred thousand components. Monolithically integrated solutions are rapidly displacing bulkier, more costly components based on discrete devices or combinations of less complex PICs.

As network capacity demands continue to escalate, integrated solutions will increasingly become ubiquitous. In order to achieve high spectral efficiency at data rates of 40Gbit/s, 100Gbit/s and above, the use of advanced modulation formats such as dual-polarization QPSK, with differential or coherent detection, is mandatory. Complex modulator circuits with in-phase and quadrature channels are required, as shown for instance in Fig. 2, and in the case of coherent detection, an optical network containing 90° hybrid couplers and multiple balanced photoreceivers is required. Monolithic solutions are attractive in these applications, in terms of cost, size, manufacturability and performance.

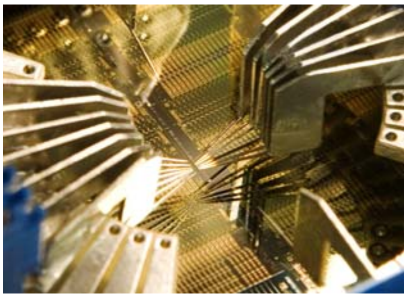


Fig. 1: Integrated InP DSDBR tunable laser-Mach Zehnder modulator devices undergoing on-wafer test

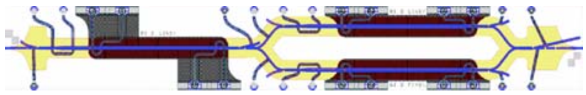


Fig. 2: RZ-DQPSK transmitter component for 40Gbit/s transponder realized in InP [3].

PIC technology is also highly attractive for multi-channel transmitters and receivers based on wavelength-division multiplexing (WDM). Fig. 3 shows a 4x28Gbit/s transmitter device featuring 'grid' tuning, i.e. all of the channels can be tuned en-bloc across the full ~40nm extent of C-band [4].

Fig. 3: Integrated tunable transmitter providing 4x28Gbit/s channels with grid-tuning.

High functionality, multi-channel, fixed-wavelength devices [5] have now been in production for some years, with applications in network nodes in WDM transmission systems.

III. CHALLENGES

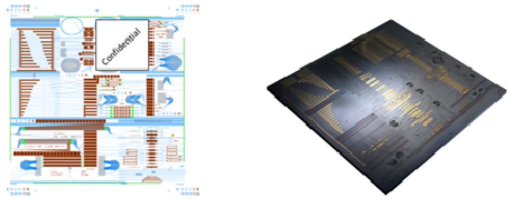
From the foregoing discussion we can readily see the importance of PIC technology within the telecommunications field. Nevertheless there are many challenges, both technical and financial [2], that face any PIC manufacturer. The fabrication processes can be complex (a tunable transmitter PIC such as those described above typically involves 5 or 6 stages of epitaxy) and, although high yields are now achieved, these devices remain demanding in terms of manufacturing expertise. The entry cost is high and the capital investments needed to maintain the necessary manufacturing infrastructure at the state of the art are very substantial. At the same time, volumes in the optical telecommunications market, although significant, are much smaller than those encountered in the silicon IC industry, which shares many of the same economic challenges. We should therefore examine whether new industrial models could be invented which could provide the basis for manufacture in higher volumes, facilitate technology access for a wider range of products and companies and thus provide the stimulus for the virtuous spiral of increased revenues and investment, lower costs and higher profitability.

IV. GENERIC INTEGRATION PLATFORMS

In order to achieve economies of scale, it will be mandatory for a wide range of products, addressing applications in different fields, to employ the same fabrication processes. Furthermore it is highly advantageous to define a generic integration platform [6], in which circuits are constructed from pre-defined building blocks (e.g. waveguides, optical amplifiers, couplers, phase shifters) contained in design libraries, rather than being designed from scratch for each new application. Sophisticated design tools will assist the designer in laying out a complex circuit based on these building blocks and in simulating its performance.

Although this is standard practice in microelectronics, it represents a radically new approach in the photonics industry. The European Network of Excellence project, ePIXnet, defined such a scenario in the early years of the present century [6] and a number of European research projects, notably EuroPIC [7] and PARADIGM [8] for InP and HELIOS for silicon photonics [9], are presently working on the task of validating this new approach.

One very attractive feature of the generic platform approach is that it facilitates the combination of different designs on a single mask set, processed in a multi-project wafer (MPW) run. This methodology is familiar in microelectronics and presently facilitated in that field by organizations such as EuroPractice [10]. An analogous way of working is now being introduced in the photonics field by the JePPIX platform for InP [11] and ePIXfab for silicon [12]. Fig. 4 shows how a set of different designs can be combined on a single mask and wafer, thereby reducing the cost for each circuit. Such an approach could widen access to PIC technology significantly and facilitate its adoption by small companies (SMEs).



Fig, 4: Sample designs in the JePPIX process: mask layout (left) and finished multi-project wafer cell (right). Illustrations c/o TU Eindhoven

Current European projects [7,8] are addressing all aspects of generic platforms in InP, from the design of the platform itself to software and design systems, and are providing experience of releasing such a platform to external designers. This work will provide a sound basis for an assessment of generic platforms as a business concept.

V. CONCLUSIONS

It is clear that PICs will continue to have a bright future for high-performance telecommunications and they show great promise for other fields, provided we can find ways to reduce entry costs, find sufficient volume in adjacent markets and thereby take this technology to higher levels of market penetration and economic viability. Present European projects are playing a vital role in exploring the potential of the generic platform approach, which could achieve just that objective.

ACKNOWLEDGMENT

The author would like to thank the partners of the ePIXnet, EuroPIC and PARADIGM projects, as well as his colleagues at Oclaro, for many valuable discussions.

REFERENCES

[1] M.J. Wale, "Photonic Integration Challenges for Next-Generation Networks", Symposium on "InP and Si Integrated Photonics: Competition or Symbiosis?" ECOC 2009, Vienna, 21 September 2009.

[2] A. Carter, "Unlocking the value of fab ownership", Compound Semiconductor, **16** (1), February 2010, pp. 34-37.

[3] C.F. Clarke, R.A. Griffin and T.C. Goodall, "Highly Integrated DQPSK Modules for 40 Gb/s Transmission", Proc. Conf. Optical Fiber Communication, 2009, paper NWD3.

[4] R. Blum, "Highly Integrated InP Laser Arrays: Closing the Gap Between Datacom & Telecom", Workshop on *Data and Telecom: Convergence of Hardware*, 37th European Conference on Optical Communication, Geneva, Switzerland, 18 September 2011.

[5] R. Nagarajan et al., "Large-Scale Photonic Integrated Circuits", IEEE J. Sel. Top. Quant. Electron. JSTQE, **11** (1), Jan/Feb 2005, pp. 50-65.

[6] ePIXnet Steering Committee, "Towards a foundry model in micro- and nano-photonics: a vision for Europe", available at www.epixnet.org.

[7] http://www.europic.org/

[8] http://paradigm.jeppix.eu/

[9] http://www.helios-project.eu/

[10] http://www.Europractice.org

[11] http://www.jeppix.eu

[12] http://www.epixfab.eu/