

# Photonics Design Automation workflow

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**Abstract**—A Photonics Design Automation workflow is discussed, in which the whole chain from initial idea to final reticle composition is supported by an integrated software tool chain.

**Keywords:** *Photonics Integration Platforms; Generic Manufacturing; Photonics Design Flow Automation; Design Rule Checking; Generic Integration Software*

## I. INTRODUCTION

In the electronics industry, the use of 'Electronics Design Automation' (EDA) is wide-spread. A foundry offers a set of building blocks (BBs), which a designer can use to create a complex device. The BBs and their combination are guaranteed to work as expected if the given design rules are respected. Software takes care of any step of the design process, from physical analysis to layout and flags any design rule violation before the final design is shipped to the foundry. Furthermore, simulation tools are integrated in or link directly into the EDA environment and assist the designer in his work.

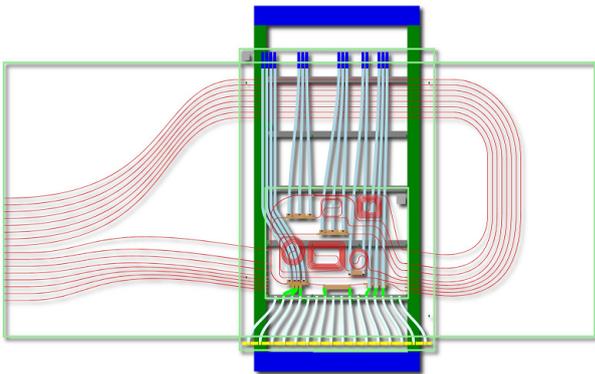


Figure 1: Example of an InP chip mounted on a silica motherboard [11] with electrical connections as it appears in the developed photonics design automation environment.

In photonics, such design kits have not been available until recently. In the European FP7 projects 'Europic' [1], 'Paradigm' [2] and 'Helios' [3] a number of European software companies have worked together to set up a Photonics Design Automation (PDA) tool set. Just like in EDA, photonic foundries define a number of building blocks, which are implemented in software ranging from mask layout through physical and circuit simulators. The circuit simulator is able to call the physical simulation software, or query a building block directly, in order to quickly simulate the response of a device.

Furthermore, it can call the mask layout software to export the circuit design into a physical mask layout.

Since most building blocks of one foundry have equivalent BBs in other foundries, many designs will be transferable from one foundry to another with only minor changes to the layout (due to differences in BB sizes and port locations), but significant changes to mask layers (due to differences in technologies and process flows). This is regularly used in practice by Design Houses such as VLC Photonics [8] and Effect Photonics [16].

This paper describes the process that any design for a fabrication run goes through, from the designer's mind to a final, realized, and packaged chip.

## II. DESIGN FLOW

A designer of a PIC (Photonic Integrated Circuit), who wants to have his design realized by a foundry, typically starts his design by modeling it in a circuit simulator. In a circuit simulator, one designs an optical circuit by placing building blocks from the foundry library with their properties into the circuit layout. The designer does not care how exactly a building block is implemented; the foundry just specifies the input / output ports and, possibly in conjunction with physical layer simulators, the wavelength-dependent scattering matrix (S-matrix) of the block. By clicking together a circuit and specifying its input and outputs, the designer can very quickly calculate the spectral response of the complete device. He can then optimize it for better functionality or for better robustness with respect to fabrication technology tolerances.

Once a satisfactory design has been created in the circuit design tool, it can be transferred, via the PDA framework, to a mask layout environment. The user specifies a die type available in the foundry and (if packaging options are available) a package. Such a combination of die type and package defines the locations of optical and electrical input and output ports. In this environment, the designer can adjust the exact layout of his design to optimize for space constraints and to make sure all connections (both optical and RF or DC electrical connections) are correct.

In the mask layout software, the designer might only be allowed to see the outline of the foundry-defined building blocks. A foundry can protect its IP by just exposing a bounding box and the locations and dimensions of access waveguides and connections for electrical signals, as shown by the private building blocks in Figure 2.

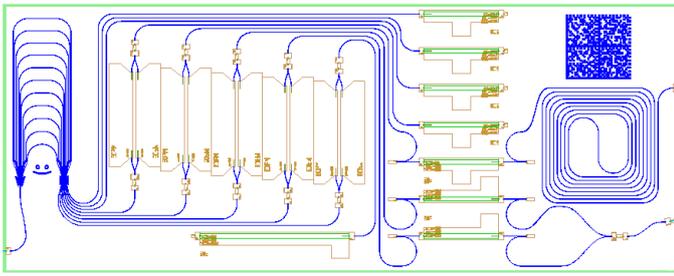


Figure 2: Mask design with bounding boxes for IP licensed building blocks. The AWG is developed by BrightPhotonics [7]

When the designer is satisfied with his mask layout, he exports it to a mask file. This process involves post processing on the mask layers that are defined by the foundry; for example, a waveguide on the final mask might have to be a little wider than designed to correct for under etch, or a final mask layer might have to be a local inversion of the designed waveguide. During the automatic mask export, the software performs design rule checks (DRC) on both the logical and mask layer levels; an example of a logical check is the radius of curvature of a waveguide, while an example of a mask layer check is whether a metallization layer and a waveguide layer overlap – or are closer than a given distance to each other.

Since the designer has no knowledge of the inner workings of a private building block, the mask files that are produced will be incomplete as the IP-protected building blocks are left open. The export process also generates a list of used building blocks and their locations. When the foundry receives designs created with the developed design environment, for example for a Multi Project Wafer run, it assembles all the mask files from the users into one reticle mask set. Furthermore, it uses the building block information supplied by the users to fill in the private building blocks in all designs with its own proprietary mask data. After this final mask assembly, the reticles can be created.

### III. FUTURE OUTLOOK

A set of re-usable building blocks that are available in foundry processes will lead to huge cost reductions. This will open up the application of photonics integration technologies to a much larger public. Instead of optimizing the fabrication technology for every specific application, the product design will be adapted to the capabilities of available, mature, high performance fabrication processes. The presented PDA environment plays a central role (see Figure 3) in the whole product and value chain from concept application to material, through design to manufacturing.

The developed PDA framework is not restricted to the software vendors setting it up and the involved foundries. Other parties can create their own plug-ins and building blocks. For example, two different Arrayed Waveguide Grating plug-ins have been created by third parties [7, 15] and are actively being used in the MPW runs designs.

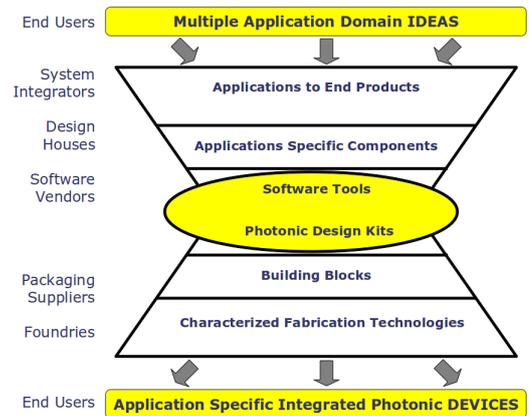


Figure 3: Photonics Design Automation as central pivot point in the 'food chain' [6].

### IV. CONCLUSIONS

The design flow as described in this paper has been applied successfully within a number of projects. MPW runs in InP [1, 2, 5], TriPleX™ [5] and SOI [4] have been run on the platform, and more than 50 designs have been successfully implemented in the past six months, for six different foundries and two packaging providers.

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