Integrated Receivers on SOI for PSK Modulation Formats

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***Abstract*— Phase coded modulation formats require the deployment of more complex receiver configurations. Waveguide integrated SOI boards are investigated to provide versatile optical functions for compact DPSK and QPSK detectors.**

Keywords- PSK, direct detection, coherent detection, SOI, hybrid integration.

I. INTRODUCTION

Novel data modulation formats such as Phase Shift Keying (PSK) modulation require receiver configurations of increased complexity, which include an optical decoder to detect and evaluate phase differences between received data bits. To handle the increasing complexity solutions by free space optics, fiber optics or planar waveguide technology are used. Integrated solutions offer the strongest potential for scalability and high volume. This requires advanced integrated devices such as delay line interferometer (DLI) and 90°-optical hybrids, which will enable the set-up for direct or coherent detection. However, advanced photonic circuits still pose challenges such as low insertion loss and low polarization dependence. In the following, a hybrid integration scheme of active InP components on silicon-on-insulator (SOI) is proposed and investigated for the examples of 40 Gbps DPSK and 40 Gbaud/s QPSK modulation format. Our approach facilitates a modular system of building high-performance receiver chips.

II. CONCEPT

A. Integration concept

Monolithic integration of all components in one material system such as InP allows to build sophisticated receivers, e.g. for coherent detection [1]. However, the increase in chip size leads to higher costs. Moreover, high performance necessitates a large number of process steps. Alternatively, we propose a hybrid integration concept using a motherboard with planar lightwave circuits (PLC) in SOI as introduced in [2]. It provides the required larger integration area for optical decoding and phase evaluation at an affordable price while high performance active components for detection and amplification are manufactured on separate InP wafers and flip-chip assembled after initial testing.

InP technology provides active components such as photodiodes (PDs) and Semiconductor Optical Amplifiers (SOAs) with low polarization dependence and high RF bandwidth. The integration of optical waveguides enables a high-speed design and operation. Practicable flip-chip integration is achieved by end-fire coupling.

PSK receivers can then be fabricated for a wide spectrum of applications using hybrid integration technology without compromise in performance. The hybrid assembly technology used here relies on AuSn flip-chip soldering.

B. SOI motherboard

The optical network is based on SOI rib waveguides (3.5 x 4 µm). SOI rib waveguides are particularly well suited for the trimming of the polarization dependence. Silicon itself does not exhibit a material birefringence, but the choice of rib geometry and cladding overlay leaves two independent parameters for birefringence tuning. This technique is used to build optical waveguide circuits with a low polarization dependency. Recently [3], state-of-the-art performance was demonstrated for the DPSK demodulators using a DLI with a low polarization dependence on SOI of 0.4 GHz polarization dependent frequency shift (PDFS) and <0.5 dB polarization dependent loss (PDL).

The same waveguide technology was used to fabricate fully passive 90°-optical hybrids [6]. The operation of the optical hybrids relies on self imaging as a result of interference between the supported modes in the multimode region. A geometry using 4µm waveguides allows to build robust devices with respect to process tolerances. Standard silicon technology allows fabrication of devices on 200mm wafers, which can accommodate an adequate number of receiver chips with increased size.

C. Active InP flip-chip components

The concept of wideband waveguide integrated PDs was deployed to enable hybrid flip-chip integration on SOI maintaining a horizontal waveguiding throughout the assembly. Previously, the PDs had achieved bandwidths of 80 GHz and beyond [4]. The diodes were grown by a one-step MOVPE process on a semi-insulating InP substrate. P-I-N-diodes employ evanescent coupling from a single mode rib waveguide.

The PDs for upside-down assembly were modified and processed with a layout regarding mechanical, electrical and optical issues for flip-chip integration. Details of the PD layout can be found in [2]. The balanced PDs for flip-chip

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integration show a responsivity of 0.5 A/W, a polarization dependent loss < 0.5 dB and a band-width > 75 GHz.

III. Experimental Results

A. *Investigation of integrated hybrids for DPSK receivers*

The increased complexity of receivers also requires new evaluation procedures. Previous to the assembly of subcomponents, critical parameters of the DLIs and the PDs are investigated by wavelength scan and polarization scrambling in order to identify remaining birefringence, PDL and imbalance [3]. After the flip-chip integration of PDs onto the SOI DPSK decoder boards (Fig. 1a), the direct measurement of the frequency bandwidth is hampered by the transfer function of the DLI. The bandwidth evaluation requires the compensation of the transfer function, following a method described in [5]. The S21 characteristics of the hybrid and the calculated o/e bandwidth are shown in Fig. 1b.

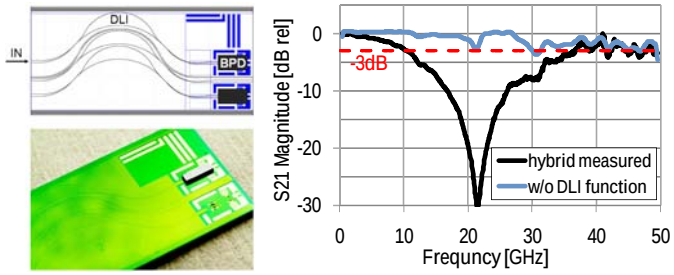

Fig 1a: DPSK receiver board. Fig. 1b: S_{21} characteristics of the assembly and calculated o/e bandwidth.

The 3 dB bandwidth of this hybrid was determined to be 30 GHz. However, the frequency bandwidth evaluation in Fig. 1b shows some ripple due to imperfections of the RF connection. Taking this into account the flattened bandwidth clearly exceeds 40 GHz.

B. *Investigation of 90° hybrids for QPSK receivers*

90° hybrids were fabricated on SOI. The hybrids are based on multimode interference (MMI) 4×4 devices, enabling fully passive operation [6].

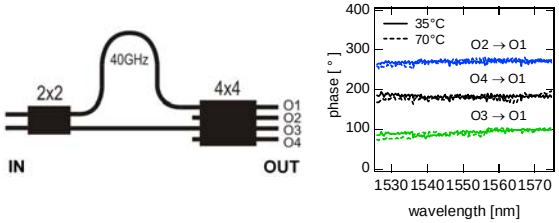

Fig. 2a: Layout of a 4x4 MMI test structure and Fig. 2b: results of phase measurements.

Fundamental performance characteristics of the hybrid are output phase relations, insertion loss, and imbalance. The evaluation of the MMI function was based on an auxiliary DLI to enable a homodyne measurement. The local oscillator signal for coherent detections was replaced by a delayed copy of the test signal itself (Fig. 2a). The phase relations between output channels were measured by wavelength scan. Fig. 2b shows the measured output phase relations across the C band. Phase deviations remained below 5°. Insertion loss and imbalance stayed below 1 dB and 0.5 dB, respectively.

IV. System Test

A DPSK receiver module comprising SOI DLI board and flip-chip integrated balanced PD was tested in a system experiment. The packaged module had a footprint of 48 x 28 mm. The RF-connection is accomplished by a coplanar line onto the PLC board between the PD chip and the RF connector. The set-up for the 40 Gbps back-to-back measurements is shown in Fig. 3a. The measured bit-error rate (BER) vs. optical signal to noise ratio (OSNR) is shown in Fig. 3b.

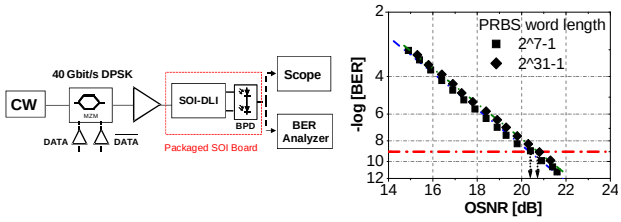

Fig. 3a: Test-bed for 40 Gbps non-return to zero (NRZ) DPSK, Fig. 3b: BER vs. OSNR for pseudo random bit sequences (PRBS) with word lengths of 2^7-1 and 2^{31}-1.

The input power was set to +19 dBm. Error free operation was achieved for an OSNR of 20.4 dB (PRBS 2^7-1) and 20.8 dB (PRBS 2^{31}-1).

V. Conclusion

Hybrid integration on SOI motherboards is a versatile technology to provide solutions for the detection of PSK modulated data signals. We have shown assembly and successful testing of a 40 Gbps DPSK receiver comprising a waveguide integrated demodulator on SOI and flip-chip integrated InP-based photodetectors.

Coherent detection with 4x4 MMIs for 90° hybrids was investigated using the same integration platform. Low phase deviations and operation over the entire C-Band enable integrated solutions of QPSK detectors. Potential receiver bandwidths of > 40 GHz permit symbol rates of up to 57 Gbaud/s and receiver designs for 200 Gbps QPSK.

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