

Vertical optical interfacing of Silicon waveguides

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Abstract—We present a novel concept and first experimental results for vertical optical interfacing of Si-waveguides on SOI substrates. The application of bent waveguides instead of grating elements assures broad spectral bandwidth and low polarization dependence. Test elements have been fabricated by using standard CMOS processing modules.

Keywords- Silicon photonics, optical interfacing, vertical coupling, butt-coupling

I. INTRODUCTION

The possibility for ultra dense integration of photonic circuits alongside with CMOS-electronic functionality has resulted in extensive research in the field of silicon photonics during the past two decades. One key issue is the interfacing between photonic waveguides/wires and optical fibers. Several approaches have been followed, each having its advantages but disadvantages as well. Grating couplers typically show good out-of-plane coupling efficiency but only narrow bandwidth and rather strong polarization dependence [1]. End-facet optical interfaces with integrated waveguide tapers exhibit both high coupling efficiency and large bandwidth but do not allow wafer scale testing of the photonic circuits since they have to be terminated on end-polished chip facets.

Here we describe a new and particularly promising option for silicon optical interfacing based on out-of-plane directed waveguide micro-bends which will eventually enable out-of-plane, low-polarization dependent and low insertion loss coupling. The new approach relies on the fact that the large index contrast between silicon (refractive index $n > 3.4$) and silicon dioxide ($n = 1.45$) or air ($n = 1$) allows the realization of waveguide bends with bending radii as small as $1 \mu\text{m}$ and negligible transmission loss [2]. So far such small bends have only been demonstrated to work in the wafer-plane, helping to route guided light along the surface of a chip or to realize minute optical ring resonators. This paper reports - to the best of our knowledge - the first application of waveguide micro-bends to out-of-plane (vertical) optical interfacing.

II. CONCEPT

Fig. 1 illustrates the schematic of the optical interfacing setup. A high index a-Si waveguide terminated by an upwards directed waveguide bend with a bending radius in the range of a few micrometers is embedded into a SiO_2 buffer, assuring optical isolation from the underlying substrate as well as mechanical stability. Light, e.g. from an optical fiber, can be

launched towards the upwards directed facet of the waveguide so that part of the incoupled light is guided through the bend section down to the straight embedded waveguide which itself may be part of a larger (extended) waveguide circuit. The bend section is either slab-like and connected to a single-mode part of the waveguide via a taper structure or single-mode as well.

First 2D simulations of these structures show the coupling efficiency to be comparable to that obtained with waveguides terminated at a chip end-facet and with a similar bandwidth of (in principle) hundreds of nanometers. The same holds for the polarization dependence. There is, however, the particular advantage of the vertical interfacing that no laborious preparation of end-facets of individual chips is needed. In addition, we do not see these structures necessarily as stand-alones. The polished wafer-surface on which the waveguides end may be used as a platform for additional structures serving to mode-match between optical fibers and the waveguides. As an example a silicon nitride top placed above the a-Si waveguide could implement such a function.

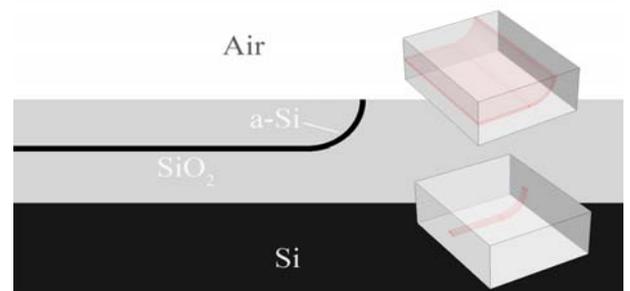


Figure 1. Schematic of the proposed design for vertical interfacing of silicon optical waveguides. The insets show a variant with a slab-like bend section (upper inset) and single-mode bend section (lower inset).

III. PROCESSING

To demonstrate the approach we fabricated test structures consisting of slab waveguides with integrated bend sections. These first test structures were fabricated on 200 mm Si wafers according to the following process flow:

First a $4.5 \mu\text{m}$ thick plasma enhanced tetraethylorthosilicate (TEOS) oxide layer is deposited on a bare Si wafer, followed by Low Pressure Chemical Vapor Deposition (LPCVD) of 200 nm silicon nitride (Si_3N_4). By i-line lithography

rectangular stripes (500 μm broad and some millimeters long) were defined and transferred into the underlying nitride by dry etching in a $\text{CHF}_3/\text{CF}_4/\text{O}_2$ plasma. For this dry etch step, a well established magnetically enhanced plasma etch equipment (MERIE) was used. The silicon nitride layer serves as a hard mask in the following wet etch step (buffered oxide etch) using hydrofluoric acid (HF). During the isotropic HF etching the silicon oxide is attacked to build a pedestal like structure underneath the Si_3N_4 -remains (cf. Fig. 2a). After the silicon nitride has been removed from the wafer using hot phosphoric acid, amorphous silicon is deposited by a disilane CVD process at 575°C . Subsequently the whole wafer is covered again with $4.5 \mu\text{m}$ plasma enhanced TEOS oxide (see Fig. 2b). A two-step Chemical Mechanical Polishing (CMP) process is applied to planarize the wafer surface (Fig. 2c) and to finally remove the unwanted amorphous silicon remains that cover the upper part of the curved waveguide sections (Fig. 2d).

The process flow as described above has been implemented using CMOS compatible technology at IHP. Fig. 2d shows the cross-section of a final structure. The waveguide core layer has a thickness of approximately 250 nm and is buried underneath $1.65 \mu\text{m}$ of SiO_2 . The lower oxide buffer measures about $2.54 \mu\text{m}$. The realized structures deviate from the theoretical form presented in Fig. 1 in that the bend sections end with a smaller angle of approximately 65° with respect to the wafer-plane. This is primarily due to the wet-etching behavior of the deposited SiO_2 in the HF solution. By adjusting the process flow to include an anisotropic dry etch step directly before the wet etch or by changing the deposition procedure completely vertical alignment is expected.

IV. EXPERIMENTS

In the experimental set-up for optical characterization we used specially designed pre-tilted fiber holders on 3-axis-translation stages to align tapered optical fibers ($\sim 3.5 \mu\text{m}$ spot size) to the waveguides. Preliminary transmission measurements were performed on typical slab waveguides with a length of approx. 2 mm. Fig. 3 shows wavelength scans of the laser-to-detector transmission as measured for the polarization controller being adjusted to maximum (state 1) and minimum (state 2) laser-to-detector transmission, respectively. The inset of Fig. 3 shows the normalized beam profile at the output facet of the slab waveguide, measured by moving the output fiber along the output facet. The laser-to-detector transmission shows an almost exponential increase with increasing wavelength of up to 17 dB over the accessible wavelength range from 1470 nm to 1570 nm which we tentatively attribute to multimode effects. The maximum laser-to-detector transmission as obtained at 1570 nm was about -54 dB for the polarization being in state 1 and -62 dB for the polarization being in state 2. The losses can be partly explained by the beam divergence inside the slab waveguide.

V. CONCLUSION AND OUTLOOK

We have demonstrated light coupling to and out of a-Si slab waveguides using upwards directed waveguide micro-bends coupled to tapered optical fibers. Further experimental investigation along with numerical simulations is currently being conducted to verify and further quantify the results as

well as to identify the individual loss mechanisms. As a next step, following the fabrication of slab waveguide structures, processing of single-mode vertical micro-bends is under way. Promising applications include economic wafer-level probing, on-surface fiber pigtailing, or even optical interfacing of (individual) functionalized nano-structures on chip.

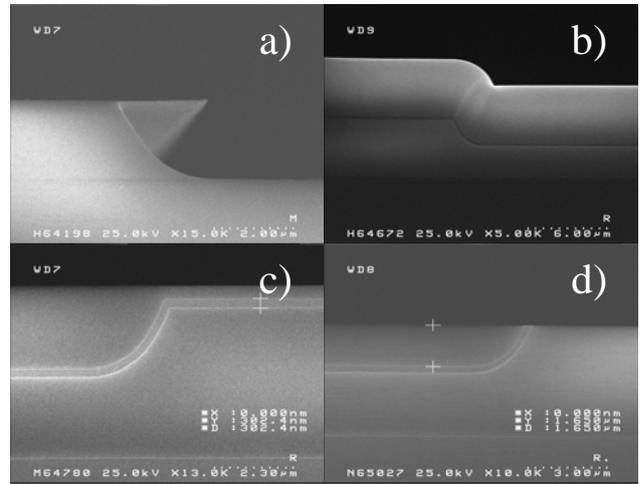


Figure 2. Si waveguide preparation process: Fig. 2a: after oxide wet etching; Fig. 2b: after 2nd TEOS oxide deposition; Fig. 2c: during oxide CMP; Fig. 2d: after a-Si CMP

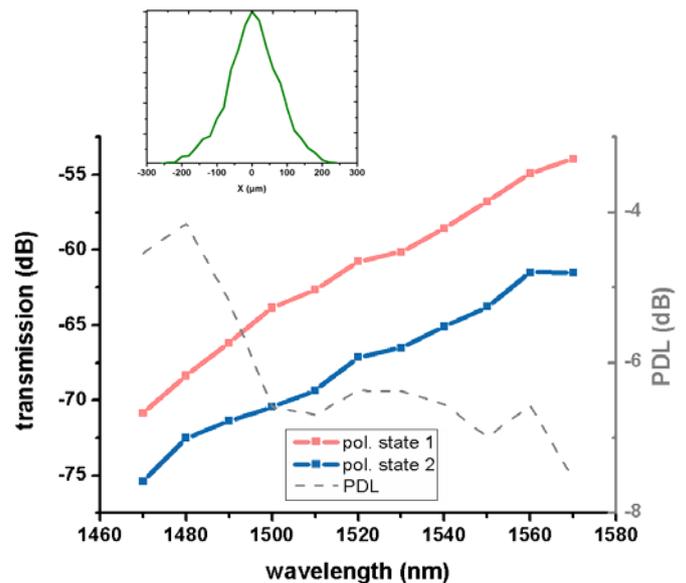


Figure 3. Laser-to-detector transmission for polarization states 1 and 2, polarization dependent loss (PDL). Inset: Transverse beam profile at output facet.

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