Integrated Photonic Circuits for Ultra-fast Sampling and Inherently Linear 6-bits Flash Quantization Based on Coherent Multi-Phase Interferometry

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Abstract—**We propose a novel 6 bits 40Gsamp/sec photonic-sampled-and-quantized flash ADC structure, based on parallel phase-domain interferometric comparisons, realizable over Si/InP (possibly hybrid) photonic integrated circuits with complexity commensurate with the state-of-the-art of photonic integration, achieving high linearity and resilience to a multitude of impairments.**

Integrated Photonics, Photonic Integrated Circuits, Modulators, Analog to Digital Conversion, Phase Measurement.

I. INTRODUCTION

Photonic sampling and quantization techniques for *Analog to Digital Converters* (ADC) with electronic interfaces have been intensely researched in the last three decades [1], motivated by the slow improvement trend in bandwidth-resolution performance of electronic ADC, and spurred by the unique advantages of photonics.

Recent PADC research has focused on the time-stretch architecture (e.g. [2]) providing spectacular performance, yet realized by bulky systems not amenable to miniaturization by means of *Photonic Integrated Circuits* (PIC), e.g. [3].

Unfortunately, progress in photonic quantization (e.g. [4-7]) has not been keeping up with the impressive advances in photonic sampling [8]. In this paper we propose a novel Photonic ADC (PADC) architecture, amenable to photonic integration, and quite distinct from all prior photonic sampling & quantization schemes, in that it is directly based on the Flash ADC principle, performing multiple comparisons in parallel, in the phase domain, based on interferometric principles.

The hitherto untapped photonic rationale is that interferometry is a fundamental optical technique excelling at generating comparisons between optical phases, put here to work in a PIC: the voltage under test is linearly converted into phase (referred to as the phase-under-test), then multiple parallel interferometric comparisons of the phase-under-test are performed against a sequence of angular thresholds (ADC transition levels). This realizes the flash principle, except that the signal under test and ADC thresholds are now optical phases rather than voltages.

The proposed compact flash PADC-in-a-PIC promises high performance (6 bits, ~4 effective bits at tens of GHz bandwidth), and is amenable to mass production over Si/InP PIC platforms due to its structure, further facilitated by its inherent tolerance to impairments and fabrication errors, stemming from phase- rather than intensity-domain operation.

Finally, while highly valuable in itself, the novel Flash PADC is not "the end game" but constitutes a stepping-stone, providing a building block in novel compound PADC architectures which we have conceived (pipelining and *Successive Approximation Register* (SAR) structures combining two or more flash PADCs), with resolutions potentially exceeding 10 bits effective (also with tens of GHz bandwidth, even without time-interleaving).

II. A NOVEL FLASH PADC ON-A-PIC

The proposed flash PADC block diagram is shown in Fig. 1 (for acronyms see the figure caption). A *b*-bits PADC requires an array of $N = 2^{b-1}$ PCs (e.g. *N*=32 for 6 bits). Each of the *N* interferometers (formed by the shared PP-PM, one of the ODCs, and its BPD), acts as a phase-detector. The *n*-th PHD amounts to an MZM with its quadrature point quasi-statically biased at $\theta^{(n)} = n\pi / N$, $n = 0, 1, ...N - 1$ (an extra $\pi / 2$ phase bias is built-in). In the *k*-th time interval, the phase-under-test $\phi_k = V(kT)\pi / V_\pi \in \{-\pi, \pi\}$ is interferometrically compared against each of the phases $\{\theta^{(0)}, \theta^{(1)}, ..., \theta^{(N-1)}\}$. The polarity of the *n*-th photocurrent sample $i_k^{(n)} \equiv i^{(n)}(kT)$ indicates whether or not $\phi_k > \theta^{(n)}$: $\text{sgn}\{i_k^{(n)}\} = \text{sgn}\{\sin[\phi_k - \theta^{(n)}]\}$. E.g. let $|\phi_k - \theta^{(n)}| < \pi$, then $i_k^{(n)} > 0$ iff $\phi_k > \theta^{(n)}$, i.e. the *n*-th PC compares the phase-under-test against the *n*-th ADC transition $\theta^{(n)}$. In the OEBE, the *N* photocurrents are TIA-amplified, sign-detected (sliced) by an array of uncoupled 1-bit ADCs, then processed by the encode-logic.

The signs assumed by the sinusoidal *transfer characteristics* (TC) (Fig. 2) describing the *N* interferometers, when sampled at the phase-under-test ϕ_k, suffice to uniquely determine which of the *M* ADC bins (quantization intervals) ϕ_k actually belongs to. Remarkably, the TC sinusoidal non-linearity is inconsequential, since the only info required in order to quantize ϕ_k (identify its ADC bin) is whether ϕ_k falls to the right or to the left of each quadrature point; as each sinusoid is odd around its quadrature point, then we just detect its sign. Hence we attain *high PADC linearity,* unrelated to the TC nonlinear shape; instead the PADC linearity is set by the C&C ability to spread the *N* quadrature bias phases $\{\theta^{(n)}\}$ at regular

angular intervals π / N over $\{0, \pi\}$. Our PADC integrated device (Fig. 1) has the following desirable characteristics:

(i): Amenable to compact and resilient *PIC realization*, e.g. over photonic integration platforms consisting of Silicon Photonics, SOI, InP, LiNb0$_3$ or combinations thereof, in particular hybrid Si/InP integration platforms.

(ii): Implements the equivalent of an electronic *flash* ADC in terms of its abstract system block diagram, performing multiple parallel comparisons of the signal-under-test (albeit in the phase domain).

(iii): Unlike in most photonic quantization systems, the signal-under-test here is not *intensity*, but is effectively *optical phase*, imparting extra resilience to the system. The phase comparisons required in the flash architecture are interferometrically performed, effectively amounting to parallel thresholding by means of an effective array of MZMs with regularly spaced quadrature points (the multiple MZMs are virtual, as physically just one pair of phase modulators – the front-half of a single MZM - is actually used).

(iv): Inherently linear: our PADC linearity is not limited by the sinusoidal interferometric TC, but is essentially set by the ability to adjust and stabilize multiple quasi-static phase-shifts (the quadrature settings of the effective MZMs in Fig. 2a) by means of slowly-varying *control and calibration* (C&C) procedures, adaptively actuated by either training sequences or by blind (decision-directed) equalization techniques.

(v): Resilient to a variety of PIC impairments and fabrication errors - this stems from the quantization action essentially occurring in the phase domain, rendering PIC performance impervious to most (but not all) amplitude imbalances, coupling ratios, amplitude fluctuations; the tolerances on the PIC fabrication are then relaxed compared to conventional intensity modulation based PADC schemes.

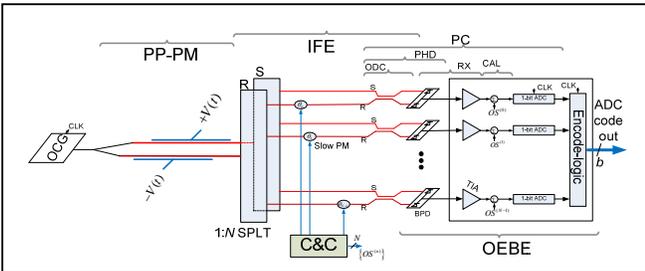**(vi):** Operates in differential (balanced) push-pull mode

Figure 1. Integrated Flash Photonic ADC system based on coherent multi-phase interferometry. OCG=Optical Comb Generator; PP-PM=Push-Pull Phase Modulators; IFE=Interferometric Front-End; OEBE=Opto-Electronic Back-End; PC=Phase-Comparator; PHD=Phase-Detector; SPLT=(N-way) Splitter; PP-PM=Push-Pull Phase-Modulator; ODC=Optical Directional Coupler; RX=Optical Receiver; BPD=Balanced Photodiodes pair; TIA=Trans-impedance amplifier; CAL=Calibration offsets section; C&C=Control&Calibration; 1-bit ADC=Slicer (sign-detector; comparator to zero). V(t) = voltage-under-test. Notice that the two 1:N splitters (drawn for clarity on top of each other) are actually laid out side by side in integrated planar lightwave circuit implementations, wherein some waveguide interconnects from the two splitters to the ODCs cross each other.
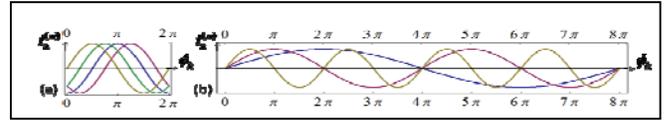

Figure 2. Transfer Characteristics (TC) : (a): TC plots of a 5-bit version of our PADC for the *N=4* PCs. (b): TC plots for a "Tayor-like" PADC based on parallel modulators [4,5], some with excessively low V_π, or serially-cascaded modulators [6]. Notice that our PADC just requires a 2π or $\pm\pi$ phase excursion, whereas Taylor-like schemes require a $2\pi N$ phase excursion.

with antipodal phase modulations and balanced photo-detector pairs), hence gaining 3 dB in shot-noise SNR, and further reducing certain common-mode impairments (see next point).

(vii): Relaxed *optical comb generator* (OCG) requirements: tolerance to pulse-to pulse intensity fluctuations, to laser RIN.

(viii): Amenable to calibration (tuning out) of most residual impairments (those which are not automatically cancelled by the phase-based amplitude-insensitive operation in balanced mode); the calibration is achieved by having the C&C module apply quasi-static controlled offsets in the electrical domain. The other C&C function is adjustment of the slowly varying control phase-shifts to ensure the system linearity.

(ix): The phase comparators (PC) count, *N*, is half as large as in electronic flash ADC: $N = 2^{b-1}$ rather than $M = 2N = 2^b$, with *b* the number of bits. E.g., a 6-bit system requires just 32 PCs rather than 64, halving the PIC complexity.

(x): Sampling rate performance: The "speed" (bandwidth) of the system is determined by that of the electro-optic modulation (up to tens of GHz at low V_π), as well as by the speed of the terminal electronic slicing operations (the array of 1-bit electronic ADC, i.e. sign detectors).

(xi): Accuracy and bandwidth performance: High-speed electronic flash ADC systems are typically unable to exceed 6 bits, our PADC being no exception (as the comparators count rises exponentially in the number of bits *b*). The *effective number of bits* (ENOB) is typically 1-2 less than the number of bits. Given the beneficial PADC characteristics surveyed above, and in particular the inherent tolerance of the architecture to impairments, we expect at least 4 effective bits at tens of GHz bandwidth.

The proposed flash PADC is valuable in itself and may further serve as a building block in compound integrated pipeline PADC structures potentially exceeding 10 bits effective.

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