An Athermal Delay Circuit Using Trenches Filled with Silicone Resin

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***Abstract*—We fabricated an athermal delay circuit using trenches filled with silicone resin that has opposite temperature dependence to the silica. It was designed for the 1-bit delay circuit for 12.5 Gbit/s differential phase shift keying receiver and it exhibits wide operating temperature range.**

Keywords- Athermal waveguide; differensional phase shift keying;

I. INTRODUCTION

Silica-based planar lightwave circuits (PLCs) are reliable, low-loss, and feature low junction loss with optical fibers, so various types have been used for optical networks. However, the temperature dependence of the silica is too large for most interference circuits like 1-bit delay circuit. So the temperature of the circuit needs to be controlled. Using Athermal waveguide we can reduce fabrication cost and power dissipation [1-3]. In this paper, we have designed and fabricated the athermal 1-bit delay circuit for a differential phase shift keying (DPSK) receiver.

II. ATHERMAL WAVEGUIDE

A. Structure of the athermal waveguide

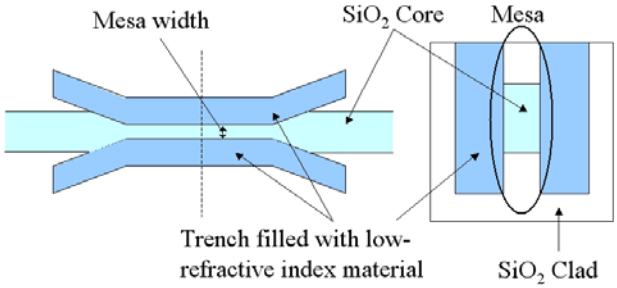

Figure 1. Structure of the athermal waveguide

The structure of the athermal waveguide is shown in Fig. 1. Trenches are fabricated along the core of the waveguide and filled with low-refractive index material [4, 5]. We used Silicone resin as a low-refractive index material. The propagation constant of the waveguide is determined by the refractive indices of the core and the low-refractive index material; their thermo-optic coefficients have opposite sign, and therefore the temperature dependence of the waveguide can be suppressed.

B. Effective index of the athrmal waveguide

The temperature dependence of the effective index of the waveguide can be described as;

$$n_{eff}(T) = A(T-25)^2 + B(T-25) + C \quad , (1)$$

where, T is temperature in degrees Celsius. A, B and C were constants calculated for mesa widths of 2.0 to 4.0 μm, as shown in Table I and II. The refractive indices of the core, the cladding layer and the resin were assumed to be 1.466, 1.444, and 1.393, and the thermo-optic coefficients of the silica and the resin were assumed to be 1.6×10^{-5} and -3.7×10^{-4}, respectively.

TABLE I. EFFECTIVE INDEX FOR TE MODE

	$A(10^{-5})$	$B(10^{-5})$	C
Normal	0.00091	1.65822	1.45632
Mesa 2.0 (μm)	0.01273	-3.76270	1.43956
Mesa 2.5 (μm)	0.00921	-1.76026	1.44493
Mesa 3.0 (μm)	0.00685	-0.62397	1.44856
Mesa 3.5 (μm)	0.00528	0.06216	1.45111
Mesa 4.0 (μm)	0.00421	0.49907	1.45296

TABLE II. EFFECTIVE INDEX FOR TM MODE

	$A(10^{-5})$	$B(10^{-5})$	C
Normal	0.00094	1.65687	1.45630
Mesa 2.0 (μm)	0.01283	-2.95334	1.44059
Mesa 2.5 (μm)	0.00907	-1.26293	1.44562
Mesa 3.0 (μm)	0.00668	-0.30314	1.44903
Mesa 3.5 (μm)	0.00513	0.27885	1.45143
Mesa 4.0 (μm)	0.00409	0.65132	1.45318

The thermo-optic coefficient of the waveguide depends on the mesa width. When the mesa width is wide, most of the light is confined in the silica core; therefore, the thermo-optic coefficient of a waveguide is positive. On the other hand, when the mesa width is narrow, some of the light is in the cladding region, and the thermo-optic coefficient is negative.

III. DESIGN OF ATHERMAL DELAY CIRCUIT

A. *Structure of 1-bit delay circuit*

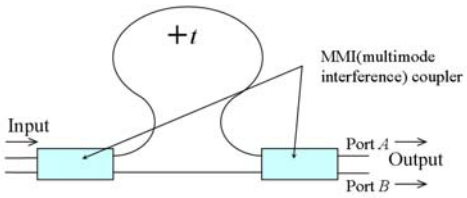

Figure 2. Schematic of 1-bit delay circuit

A schematic of the 1-bit delay circuit for the differential phase shift keying (DPSK) receiver is shown in Fig. 2. The time delay is set to the symbol period, *t*. In DPSK signaling, the symbols [0] and [1] are assigned to the phase difference between successive bits. The output light power from the output port is determined by the phase difference between the successive bits. When the phase difference between the successive bits is π, the light is output to port *A*., whereas when the phase difference is 0, the light is output to port *B*. Finally, a balanced receiver converts the output light into an electrical signal.

B. *Temperature dependence of the 1-bit delay circuit*

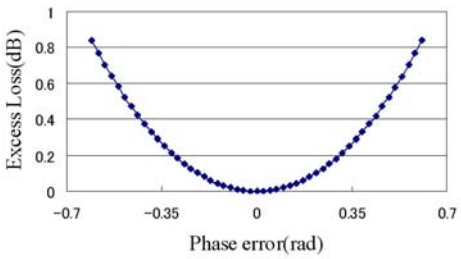

Figure 3. Excess loss caused by phase difference error.

Figure 3 shows the excess loss caused by the phase error to the second MMI. The optical length difference in the asymmetric MZI for a 12.5 Gbit/s DPSK signal is about 24 mm; therefore, the temperature change can easily lead to a phase error and the associated excess loss. The phase error range for excess loss of less than 0.5 dB is -0.45 rad to 0.45 rad.

C. *Design and Fabrication of Athermal 1-bit delay circuit*

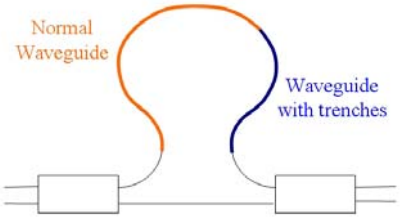

Figure 4. The athermal 1-bit delay circuit

We use normal waveguide and waveguide with trences for 1-bit delay, as shown in Figure 4. The mesa width of a waveguide with trenches is 2.0μm. We calculated the ratio of the length of both waveguides for athermal condition. Table III shows calculation results. The structure of athermal 1-bit delay circuit that we fabricated is shown in Fig. 5.

TABLE III. WAVEGUIDE LENGTH

	The Length of Normal Wavguide (mm)	The Length of Wavguide with Trench (mm)
TE mode	11294	5235
TM mode	10381	6153

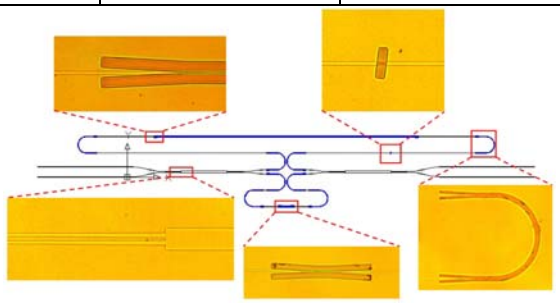

Figure 5. Structure of 1-bit delay circuit.

IV. EXPERIMENTAL RESUITS

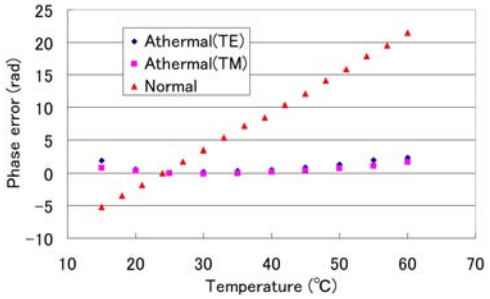

Figure 6. Temperature dependences of fabricated 1-bit delay circuits.

The experimental results of 1-bit delay circuits that we fabricated are shown in Fig. 6. By applying the athermal waveguide, the temperature range for the excess loss of less than 0.5 dB was extended from 1.5 (Normal) to 25.0 degrees (TE) and 30.0 degrees (TM).

V. CONCLUSION

We proposed a novel athermal waveguide structure. We also fabricated a 1-bit delay circuit for the 12.5 Gbit/s DPSK receiver, which had a wide operating temperature range.

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