All-Optical Memory Operation for 20-Gb/s PRBS RZ and 40-Gb/s NRZ Signals Using 980-nm Polarization-Bistable VCSEL

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Abstract—**Ultrafast all-optical memory operation was experimentally demonstrated using a 980-nm polarization-bistable vertical-cavity surface-emitting laser. 1-bit data signals were arbitrarily sampled and memorized from a 2^6-1 pseudorandom bit sequence return-to-zero signal at 20 Gb/s and a 6-bit non-return-to-zero signal at 40 Gb/s by AND gate and memory functionalities.**

Keywords-VCSEL; polarization bistable switching; optical buffer memory

I. Introduction

All-optical buffer memories are desirable as key elements of all-optical packet-switched networks. We previously proposed an optical buffer memory with shift register function consisting of a two-dimensional array of polarization-bistable vertical-cavity surface-emitting lasers (PB-VCSELs) [1]. We have demonstrated that such buffer memory consisting of four VCSELs can store and regenerate 4 bits in a 1550-nm range [2]. The fastest 1-bit buffering achieved so far has been for 10-Gb/s return-to-zero (RZ) signals in a 980-nm range [3].

In this presentation, we report 1-bit memory operation of 20-Gb/s RZ signals and 40-Gb/s non-return-to-zero (NRZ) signals using a 980-nm PB-VCSEL. We have succeeded in memorizing an arbitrary bit of the pseudorandom bit sequence (PRBS) data signal as long as 2^6-1 bits at 20-Gb/s. In 40-Gb/s operation, we have achieved memorizing each bit of 6-bit NRZ signals. These are the fastest operation of optical bistable flip-flop memories to the best of our knowledge.

II. Principle

A PB-VCSEL has a square mesa structure and has two lasing modes with polarization directions orthogonal to each other (0 and 90°). Since one of the two modes suppresses the other through cross gain saturation, the VCSEL stably oscillates with one of these polarizations. By injection of a control light with sufficient power and at the polarization direction orthogonal to that of the lasing mode, we can switch the lasing polarization of the VCSEL as shown in Fig. 1.

This research was supported in part by the Strategic Information and Communications R&D Promotion Programme (SCOPE) and by the Ministry of Education, Culture, Sports, Science, and Technology of Japan, Grant-in-Aid for Scientific Research (B) (21360034).

The 1-bit memory function is achieved as follows (Fig. 2). The 90 or 0° polarization state of the PB-VCSEL is used to store the "0" or "1" of the target bit in the data signal, respectively. A data signal with 0° is injected into the VCSEL. The injection power of the data signal is set to less than the polarization switching threshold of the VCSEL. We also inject a set pulse with 0°. If the set pulse is injected together with a "1" data pulse and the combined power of the data pulse and the set pulse exceeds the polarization switching threshold, the polarization state of the VCSEL switches from 90 to 0°. Therefore, the polarization state of the VCSEL reflects the "0/1" of the target bit in the data signal. The stored target bit can be read out at any timing using an optical gate device.

III. Operating Conditions of Memory

As we increase the data rate, the temporal width of each data pulse and set pulse needs to be shortened. We then need higher injection power for these pulses to obtain polarization switching. When the bit length of the data signal becomes long,

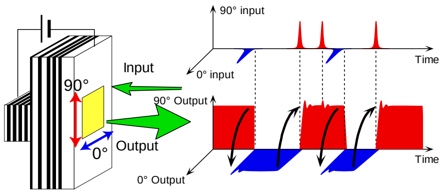

Figure 1. Polarization bistable operation by injection of optical pulses in a VCSEL.

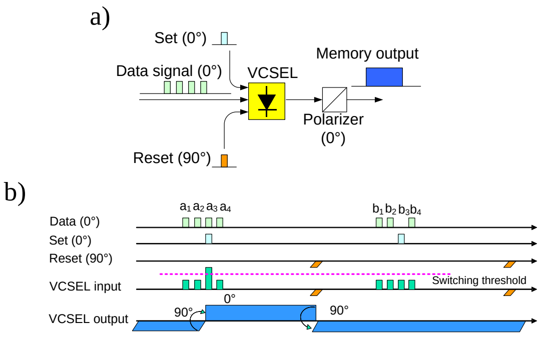

Figure 2. 1-bit buffering using a PB-VCSEL. a) Implementation and b) Timing chart.

change in the number of carriers in the active region of the VCSEL, caused by each data pulse, accumulates and causes undesired polarization switching even without set-pulse injection. One solution for this problem is to detune the carrier frequency of the data signal f_{data} from the oscillation frequency of the VCSEL f_0 [3]. Since larger frequency detuning Δf ($= f_{data} - f_0$) requires higher signal power P_{data} for polarization switching to occur, it is important to grasp the conditions for memory operation without errors in the Δf - P_{data} relation.

We performed a numerical simulation of the polarization switching using a two-mode rate equation model in order to obtain the operation conditions. We calculated two criteria for the signal power P_{data} as functions of Δf. The first was the threshold for the polarization switching to occur with injection of a data pulse and a set pulse. This curve provides the lower limit of P_{data}. Here, the data pulse power and the set pulse power were assumed to be equal. The wavelength tolerance of the input optical pulse was wider on the longer wavelength side. The second criterion was the switching threshold for long-bit data pulses (2^6-1 bits, PRBS) without a set pulse. This curve provides the upper limit of P_{data}. In our simulation for a 20-Gb/s data signal, resonant structures appeared in the upper limit curve at around -20 and -15 GHz due to the sidebands of the input data signals and the relaxation oscillation. Since the upper limit power becomes larger than the lower limit power for $\Delta f < -22$ GHz, memory operation without errors can be expected at this condition for 20-Gb/s PRBS RZ signals.

IV. All-Optical High Bit-Rate Memory Operation

We performed 1-bit memory operation for a 20-Gb/s PRBS RZ data signal using an InGaAs/GaAs VCSEL with a square mesa of 6×6 μm^2 in a 980-nm range [4]. The bias current was set to about 9.28 mA. The output power of the VCSEL was about 430 μW. Optical data signals and optical set and reset pulses were generated by tunable external cavity laser diodes and $LiNbO_3$ modulators. The input signal to the VCSEL was monitored using a sampling oscilloscope, while the VCSEL output waveform through a polarizer was monitored using a photodiode and a digital storage oscilloscope.

An example of the memory operation for a 2^6-1-bit PRBS data signal is shown in Fig. 3. For three successive groups of data signals, three set pulses were positioned to sample "1", "0", and "1" data (Fig. 3 b). When the “1” data pulse and the set pulse were injected simultaneously, the polarization state of the VCSEL switched from 90 to 0° (Fig. 3 c). The frequency detuning Δf of the data signal against the lasing wavelength of the 0° polarization mode was set to be about -23 GHz. The peak power of the data signal and set pulses were 250 and 190 μW, respectively. This data signal power was lower than the VCSEL output power. Thus, this all-optical memory operation has an optical gain even for such a high data rate. Without changing the power and the wavelength, i.e., by only changing the timing of the set pulses, we have successfully demonstrated sampling of 2^6-1-bit PRBS data. These results show the ability of the current PB-VCSEL memory to handle RZ data signals of 20 Gb/s.

We also examined memory operation for 40-Gb/s NRZ signals. In the NRZ data signal, because the set pulse interfered with the pulse tails of the adjacent bits of a target bit, the difference in the optical power of the "0" or "1" sampled bit became indistinct. Despite this problem, we have achieved the memorization of each bit of NRZ signals with a 6-bit length as shown in Fig. 4.

V. Conclusion

We have demonstrated all-optical 1-bit memory operation for 20-Gb/s PRBS RZ signals and 40-Gb/s NRZ signals using a PB-VCSEL in a 980-nm range for the first time. A 1-bit data signal was arbitrarily sampled and memorized from the 2^6-1-bit, 20-Gb/s data signals and 6-bit, 40-Gb/s data signals by changing only the time position of the set pulses.

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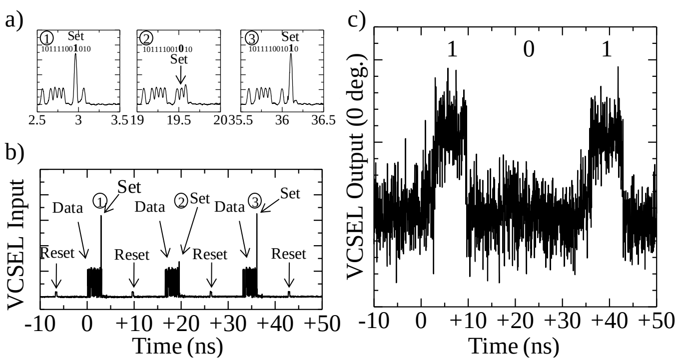

Figure 3. Memory operation for 20-Gb/s, 2^6-1 bit PRBS RZ signals.
a) Magnified VCSEL input, b) VCSEL input, and c) VCSEL output.

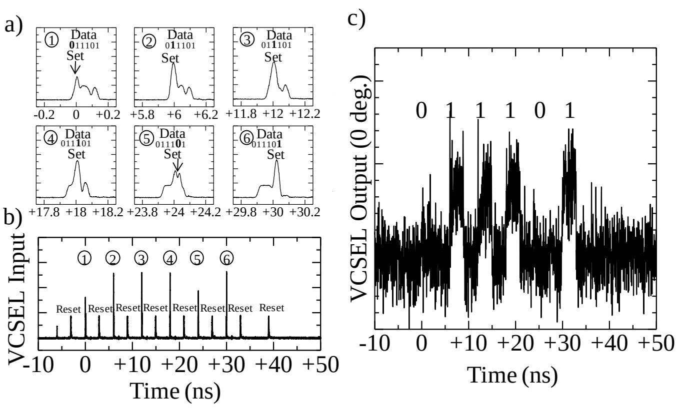

Figure 4. Memory operation for 40-Gb/s, 6-bit NRZ signals.
a) Magnified VCSEL input, b) VCSEL input, and c) VCSEL output.