Fast Reconfigurable Cyclic Router Using Semiconductor Optical Amplifier Gate Array

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Abstract— **A fast reconfigurable monolithic wavelength router with highly compact semiconductor optical amplifier gate arrays is proposed and demonstrated. Time and wavelength multiplexed data is dynamically routed with a power penalty of 3.0dB for guard times as low as 2ns.**

Keywords: Optical communication, Wavelength division multiplexing, Tunable filters, Semiconductor optical amplifier

I. INTRODUCTION

Nanosecond time-scale, wavelength-tuneable, optical filters offer an important enabler for a wavelength agile networking in metropolitan area telecommunications [1], interconnection systems [2] and access networks [3]. However, cost and energy consumption place stringent demands on the required hardware. Photonic integration can reduce the assembly complexity and remove unnecessary losses from fiber to chip interfaces. Arrayed waveguide grating (AWG) cyclic routers in particular offer a manufacturable and highly scalable route to reconfigurable networking. However, most work has required their combined use with wavelength tuneable transmitters or wavelength convertors. Recently, fast re-configurability in AWG based tunable filters has been made possible through electro-optic phase tuning [4]. Wideband unicast operation has been demonstrated but complex analog control is required.

In this work, we propose a novel digitally controlled, monolithic nanosecond re-configurable wavelength router consisting of multiband cyclic AWG integrated with a highly compact SOA gate array. Power penalty for the routed data is studied for both static and dynamically reconfigured operation. Nanosecond re-configurability for very short guard bands is analyzed by means of full bit error assessment to quantify fast reconfigured circuit performance.

II. DESIGN AND FABRICATION

The reconfigurable wavelength router consists of a highly compact 4x4 cyclic AWG with densely integrated array of four SOA gates. The device has been fabricated using an active-passive re-grown epitaxy [5]. The microscope image in figure 1 shows the functional part of the circuit. The input on the top-right is split using cascaded 1x2 multimode interference couplers to the four compact SOA gates. Each SOA gate is 140µm in length and is angled at 12 degrees relative to the active island length. These SOA gates are accommodated within one single active island of 30µm x 750µm, as shown in inset of figure 1.

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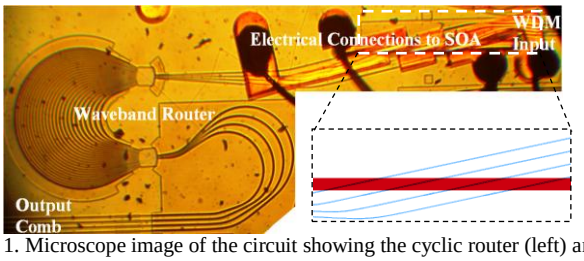

Figure 1. Microscope image of the circuit showing the cyclic router (left) and the gate array (upper right). (Inset) Mask layer representation of the four SOA gates across the active region

Wide shallow etched waveguide widths of 3µm are used for the SOAs and the 2µm widths are used for passive shallow etch waveguides. Waveguide tapers and shallow to deep waveguide transitions are implemented each side of the active island. Deep etched low radius curved waveguides allow for further circuit size reduction. The total circuit area is less than 5mm^2, including the waveguide fan-out for the fiber interface. Input and output waveguides are angled at 7 degrees to the cleaved facets for reduced reflections. Lensed fibers are used for fiber-chip coupling.

The circuit transfer function is evaluated by biasing one of the SOA gate at 50mA and measuring the amplified spontaneous emission at the input and each of the four outputs. The four output side spectra are overlaid in figure 2 for SOA gate 1 enabled. The free spectral range is five times the channel separation, leaving one band unconnected for each free spectral range. A uniform spectral performance with 2dB variation is observed across the measured 100nm bandwidth. The unfiltered spontaneous emission from the input side is also shown with a variation of under 4dB over the 100nm measurement range. Selective electrical biasing within the SOA array enables a reprogramming of the transfer function allocating wavelength comb to each of the output ports.

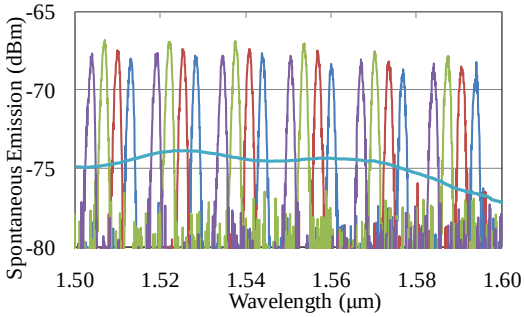

Figure 2. Cyclic router transfer function for SOA 1 enabled. Overlaid spontaneous emission spectra to the input and the four outputs.

III. Dynamic Switching Characteristics

The experimental arrangement to study the dynamic optical routing is shown in figure 3(a). Firstly, the assessment of switching performance of the SOA gate is performed. Two multiplexed wavelength channels at 7dBm (in fiber) each are input to the device. The two wavelength channels are individually routed to the same outport by sequentially changing the bias states for SOA gates 1 and 2.

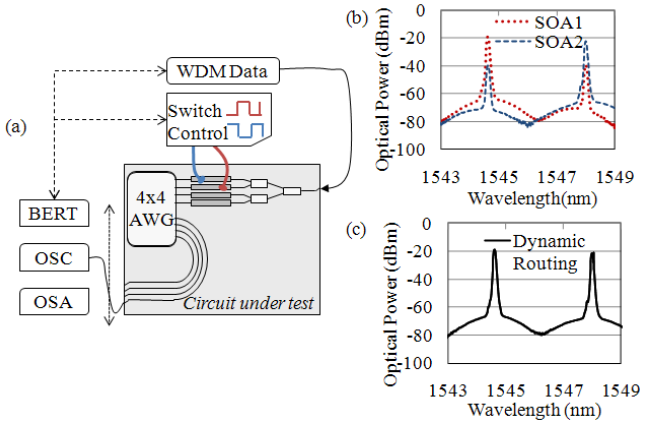

Figure 3. (a) Dynamic routing experiment, (b) For SOA1 and SOA2 on, (c) SOA1 and SOA2 alternating. (0.1nm resolution bandwidth)

Extinction ratio is measured for dc bias conditions for individual SOAs at 40mA.The output is measured on the optical spectrum analyzer. As shown in figure 3(b), extinction ratios of greater than 15dB are achieved for both switch states. Figure 3(c) shows the output spectrum when the SOAs are biased using 0 to 2V complementary square wave signal for the fast reconfigurable routing experiments.

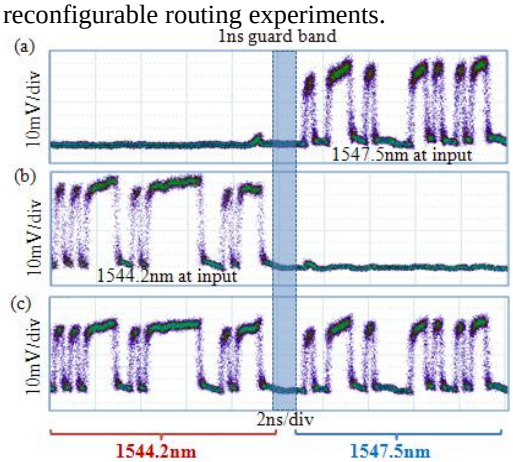

Figure 4. Fast reconfigurable routing monitoring the circuit output (a) Only channel 1547.5nm at input (b) Only channel 1544.2nm at input (c) Channels 1544.2nm and 1547.5nm at input.

The impact of nanosecond switch transitions on data integrity is studied with data at 3Gbit/second on two different wavelength channels. Two tuneable lasers are multiplexed and modulated with the same pseudorandom sequence of 2^{15} -1 bit length data. These are input to the wavelength router. The switch state is reconfigured at the rate of 5.7 kHz with 1ns electronic transition times. The oscilloscope traces in figure 4 shows the optical data during switch reconfiguration. Output port 1 is monitored for the periodically gated router for the two wavelengths individually input (a) and (b) and then simultaneously (c). The time traces show that the data sequence is transmitted only for the on-state of the corresponding SOA gate. For the off-state, the transmission is suppressed. When both the wavelength channels are present, a continuous data sequence is received as shown in figure 4(c). The oscilloscope trace shows a stable transition between wavelength channels as the circuit is reconfigured with no evidence of ringing or overshoot. The figure also shows a guard time of less than 2ns between the wavelength packets thus enabling very high link utilization.

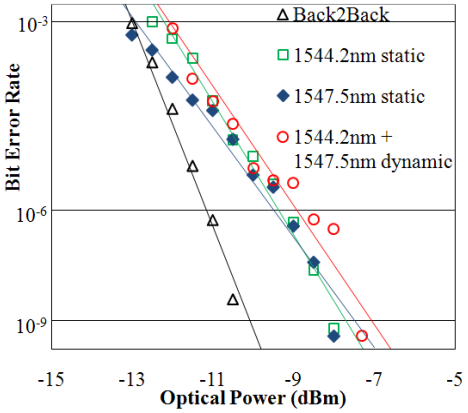

Figure 5. Power penalty assessment for all received bits, switching between 1544.2nm and 1547.5nm.

Bit error rate measurements for the received static and dynamically routed optically time multiplexed data are performed and shown in figure 5. No clock recovery is performed for the synchronized data streams in this study. No circuit dependent transient degradation is observed. Power penalty of 3.0dB is observed which is only marginally higher than the values measured for static operation.

IV. Conclusion

A gated cyclic wavelength router with nanosecond timescale re-configurability is demonstrated for the first time. The highly compact SOA gate array provides digital control and the use of cyclic router enables an intrinsically scalable architecture. A power penalty of 3.0dB is observed for both static and for dynamic wavelength routing.

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