A Compact Lossless Integrated 16×16 QW SOA Switch

H. Wang, A. Wonfor, R.V. Penty, I.H. White
Centre for Photonic Systems, Electrical Engineering Division, Engineering Department, University of Cambridge, 9 JJ Thomson Avenue, CB3 0FA
Cambridge, UK
Hw288@cam.ac.uk

K.A Williams
Technische Universiteit Eindhoven, P.O. Box 513, 5600 MB
Eindhoven, The Netherlands
k.a.williams@tue.nl

Abstract — **A monolithically integrated 16×16 Quantum Well Semiconductor Optical Amplifier switch is demonstrated. The switch has a 2dB facet-to-facet gain, a mean power penalty of 3dB and worst path power penalty < 5.5dB operating at 10Gb/s.**

Keywords-SOA;Optical switch

I. INTRODUCTION

The use of photonics for switching applications has become increasingly necessary owing to the demand for optical networks able to rapidly re-route signals between moderate numbers of input and output ports in new applications such as datacenters [1]. However, current optical switches using MEMs technology and the like have limited reconfiguration speed [2]. Semiconductor optical amplifier switches have the ability to switch on nanosecond timescales and have therefore undergone much development, with 8×8 port switches being reported [3]. However, these are realised with multiple integrated 1x8 switching elements which are separately packaged and require fibre interconnections and timing synchronization. To meet the energy and cost points for high capacity switching, integrated devices with port counts of at least 16×16 are needed for practical system applications [4]. It has been shown that 16x16 port counts can be achieved using cascaded 4x4 devices with fibre interconnections [5]. In this paper, therefore we report the first monolithically integrated 16×16 port SOA based optical switch, incorporating ~1100 individual components. The switch is re-arrangably non-blocking and has a chip area of only 6.3mm×6.5mm.

II. DEVICE DESIGN

The switch is based on a 3-stage hybrid Clos-Tree structure, which has three columns of four 4×4 port switch building blocks being connected by two fixed shuffle networks. Each of the 4x4 switching elements contains its own input and output shuffle networks and 16 SOA gates, as shown in Figure 1. In this all active switch, the waveguides in each shuffle network are forward biased to result in only a small loss between successive SOA gates. The SOA gates provide routing functionality and sufficient gain to allow lossless operation of the entire switch.

An integrated SOA switch should be compact with minimized internal loss, allowing the SOA gates to operate in a low gain regime, in order to minimize distortion and the build up of amplified spontaneous emission (ASE) noise. Therefore, the total length of the waveguides, the split and combine loss, and the number of cascaded SOA gates should be kept to a minimum. The use of beam splitters and beam turning components introduce excess losses, and hence the number of these components must also be minimized.

Table 1 shows that the 3-stage hybrid Clos structure used in this work requires the lowest number of gating SOAs and a modest number of SOA cascading stages for a re-arrangably non-blocking integrated 16x16 switch [6]. The tree architecture uses many SOAs which, whilst not cascaded, must overcome large split/combine losses. A Benes network based on 2x2 switches has a low loss per stage, but must cascade many SOAs and thus suffers from a low input power dynamic range.

TABLE I. COMPARISON OF SWITCH ARCHITECTURES FOR 16X16 PORT COUNT

Switch architecture	No. of SOA gates	No. of cascading stages	Max No. of SOA gates in each stage	Splitting loss per stage
Tree	256	1	256	24dB
Benes	224	7	32	6dB
3-Stage hybrid Clos-Tree	192	3	64	12dB

III. DEVICE IMPLEMENTATION

The switch used for this demonstration is fabricated from all active material with a 6 QW AlGaInAs active region, grown on an InP substrate, and operates with a gain peak around 1550nm. The chip layout is shown in Figure 1(a) and (b).

The shuffle network is constructed from 2μm wide shallow etched ridge waveguides, with an etch depth of 1.84μm. This relatively narrow waveguide width enables short taper lengths, where necessary for compatibility with etched turning mirrors and splitters, described later. This therefore reduces the overall path length and allows a compact switch to be developed. The SOA gates are 4μm wide shallow etched waveguide and 1mm in length (Fig. 1(c)). Adiabatic tapers are used to interface between the 2 and 4 μm waveguide widths. Thus a compact switch with dimensions of 6.3mm×6.5mm can achieve high extinction ratio and low system crosstalk.

In order to make the chip as compact as possible, 45 degree total internal reflection (TIR) mirrors (Fig 1(d)) are used to turn

the light to a perpendicular waveguide, rather than curved waveguides. These mirrors are 3.16μm deep etched and connected to 2.4μm wide waveguides on each side. The waveguides are then tapered back to 2μm. Two types of beam splitters are used in the shuffle networks, side splitters (Fig. 1(e)) and T-type splitters. They have similar structure to the beam splitters used in [7] and [8] respectively. Waveguides are linearly or parabolic tapered to the splitters. TIR mirrors are also used inside the splitters to the route half of the light to the perpendicular side waveguide. A full angle of 1 degree is used for all the linear tapers on the switch.

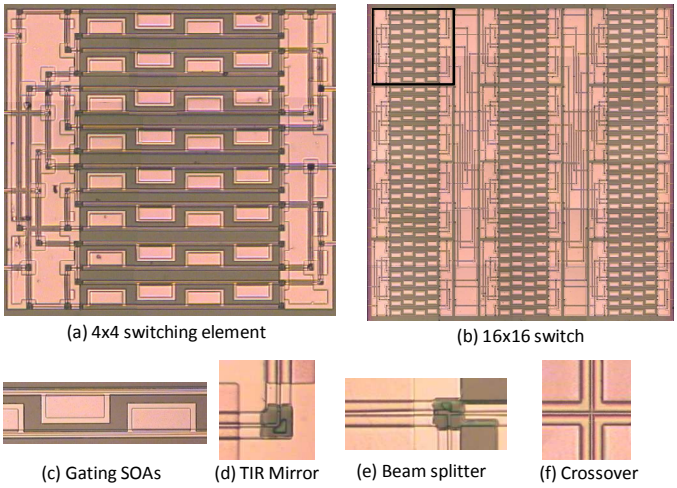

Figure 1 (a) shows a 4x4 switching element. 12 such elements are used in the 16x16 switch (b) . Key building blocks for the switch are (c) gating SOAs, (d) TIR mirrors, (e) and beam splitters and (f) waveguide crossings.

The current switch is re-growth free i.e. without active-passive interfaces. It is believed that the inclusion of, for example, passive shuffle networks would reduce ASE, nonlinear distortion and power consumption. As can be seen from figure 1, each path has three gating SOAs and goes through eight shuffle sections. Each specific input to output path on the 4×4 switch elements has a fixed length, ranging from 1.9mm to 3.35mm. Each of the two main shuffle networks has 16 paths, whose lengths are between 0.625mm and 4.225mm. As the switch is re-arrangably non-blocking, there are 4 different possible paths for each specific input to specific output, i.e. through the first to fourth 4×4 switch element in the second column. Therefore, the possible path lengths vary from 6.95mm to 16.8mm, while the shortest possible path for specific input to output pairs are range between 6.95mm and 12.7mm. Most of the paths have 13 mirrors, 12 beam splitters/combiners and a minimum possible length of less than 10mm. The switch contains 192 gating SOAs, 288 beam splitters/combiners, 424 deep etched turning mirrors and 210 waveguide crossings, a total of 1114 functional components integrated onto the same chip.

IV. EXPERIMENT DETAILS AND RESULTS

The switch is mounted on a thermo-electric cooler and operated at 15°C, with lensed fibres used to couple light on and off the chip. The switch is operated with selected gating SOAs biased between 0 (OFF) and 100mA (ON). This ensures good crosstalk performance. The shuffle networks inside the 4×4 switch elements are driven at 450mA, while the two large intermediate shuffle networks are each biased at 1000mA. This drive current is equivalent to 750mA per path. For this drive current, the switch has a facet-to-facet gain of >0dB at 1557.5nm for all tested paths with fibre coupling losses measured to be 4dB per facet. The TIR mirror loss has been measured to be 4dB. Optimisation of the design is expected to improve this. The 1dB on-chip output saturation power is -11.5dBm with a 3dB spectral bandwidth of >9nm.

Routing measurements are performed using a 10Gb/s 2^{31}-1 PRBS signal from a Mach-Zehnder modulator and an optically pre-amplified and filtered receiver. The switch output has an in-band optical signal-to-noise ratio (OSNR) of > 14.5 dB. The BERs for several selected paths are shown in figure 2. The switch operates with a power penalty of 5.5dB at a BER of 10^{-9} for the longest path (16.7mm). However, each input to output port pair has 4 possible paths and controlled re-arrangement of the switch can normally avoid this long path and keep the majority of path lengths to around 10mm or less. The shortest path and two paths which have average lengths are tested and show a minimum power penalty around 2.5dB.

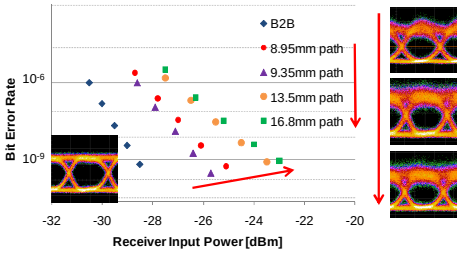

Figure 2 shows bit error rates and eye diagrams for selected paths, with red arrows showing the inceases in path length.

V. CONCLUSIONS

A monolithically integrated 16×16 SOA switch is demonstrated. The switch is compact and lossless. Routing of a 10Gb/s signal and error-free operation for different path lengths, including the shortest and longest, is achieved. The switch has a minimum power penalty around 2.5 dB, showing its potential for high speed switching applications such as packet switching.

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