Switching Ultrahigh Line-rate Optical Data in a Monolithic Multistage Interconnection Network

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Abstract—**A monolithic multistage interconnection network with minimum two and maximum four stages of cascaded crossbar switches is designed, fabricated and demonstrated. Record ultrahigh data line-rates of 160Gb/s are dynamically switched between paths exploiting the high 43.4dB extinction ratio and optical signal to noise ratio of 41.7dB/0.1nm.**

Keywords- Monolithic Integration; Optoelectonic Switching

I. INTRODUCTION

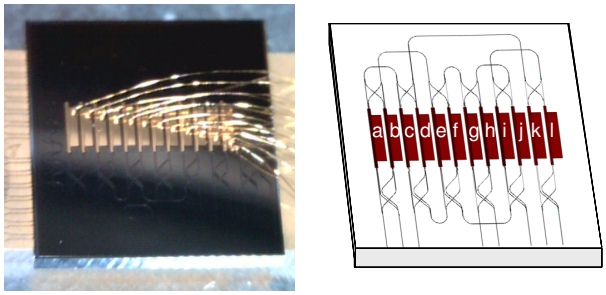
The increasing demand for high-capacity data transfer with increasing number of network connections is driving research into large capacity photonic switching systems. Nanosecond-switched, broadband semiconductor optical amplifier (SOA) based circuits have received particular attention owing to the promise of low control complexity and monolithic integration. Higher serial line-rates per wavelength offer a route to reduced inventory, simplified network management and payload-agnostic routing. Important energy savings are also anticipated as line rates increase in ultrabroadband photonic circuits. However there is little understanding of the limits to serial data rates in such monolithic multistage interconnection networks.

In this work we study, for the first time, the switching behaviour of an intrinsically scalable optoelectronic monolithic multistage interconnection network. Nanosecond timescale reconfigurable operation is demonstrated for the first time at 160Gb/s.

II. PHOTONIC INTEGRATED CIRCUIT

A. Circuit

The four input, four output multistage optoelectronic switching circuit is implemented on an active-passive regrown InGaAsP/InP epitaxial multiproject wafer [1]. The InGaAsP/InP multiquantum-well active layer is designed for 1550nm operation. Twelve active islands with area 30 µm × 1000 µm are defined on a 250 µm pitch within a larger passive waveguiding area. Fig. 1a shows a photograph of the circuit attached to a gold plated AlN subcarrier. Wire bonds connect each of the electrodes. Fig. 1b explicitly shows the implemented waveguide and electrode arrangements. Pairs of SOA gates are placed within each of the twelve active islands for enhanced integrated density. Each active island is invidually addressed using the twelve rectangular electrodes visible in the centre of the circuit. The total circuit area is implemented within chip dimensions of only 4.3mm × 2.8mm.



a) b)

Fig. 1. a) Microscope photograph of the monolithic multistage interconnection network. b) Schematic waveguide layout.

B. Architecture

The multistage interconnection network allows an increase in the number of network connections while using identical 2x2 crossbar switch cells. In this work, an N-stage planar network [2] is implemented with our previously demonstrated two-electrode crossbar switch concept [3], which is now configured for active passive integration. The four input and four output waveguides are placed at the front facet and connect to the row of crossbar cells across the centre of the circuit. Each crossbar switch has four SOA gates which are configured to occupy only two active islands. The two electrodes define either cross or bar state. Six such crossbar switches are interconnected by means of deeply etched 100 µm radius curved waveguides integrated within the low-loss, passive-waveguide shuffle network. Waveguide crossings are implemented with shallow waveguides to reduce path dependent crosstalk. Splitters and combiners are implemented with multimode interference couplers. Eleven of the sixteen paths are successfully implemented despite a wiring error.

III. EXPERIMENTS

Operating fibre to fibre loss is measured to be –13.7dB and –14.0dB for the two stage paths studied here. Losses are dominated by the 6.0dB fibre to chip coupling loss leading to estimated on chip losses of only 1.7dB and 2.0dB. Net chip gain is feasible, but facets are not anti-reflection coated, and therefore modest operating currents are selected to avoid spectral ripple and subsequent signal impairments.

The chip has been fabricated on the Photonic Integration Platform JePPIX. A. Albores-Mejia acknowledges the support of CONACyT-Mexico.

Switching is initially characterised in terms of a static extinction ratio. Optical transmission is compared for two bias currents at one SOA gate electrode: low state 0mA and high state 120mA. A polarisation-aligned, continuous-wave signal is input with 3dBm (in-fibre) power at 1550nm. Fig. 2 shows the measured extinction ratio of 41.2dB. Optical signal to noise ratio is measured to be 39.5dB/0.06nm. These good values are indicative of high gain and low loss within the circuit.

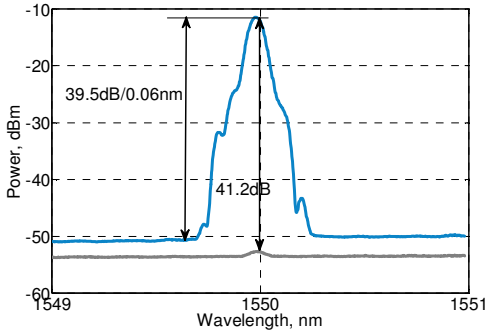


Fig. 2. Switching extinction ration and OSNR for a polarization optimized CW input signal.

High serial line rate transmission is studied by inputting 160Gb/s signals into two different ports and assessing via the same output. The experimental arrangement is shown in figure 3. The switch is controlled with a combination of current sources and fast transition pulse generators clocked at 2.6MHz.

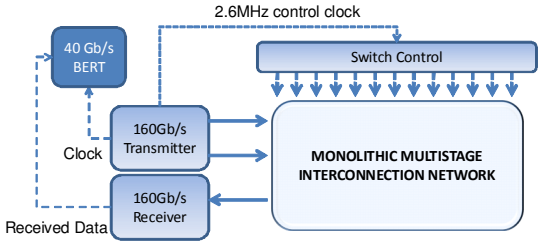


Fig. 3. Experimental setup for 160Gb/s data routing.

The 160Gb/s serial data is an aggregate of sixteen optically time division multiplexed 10Gb/s tributary channels. An aggregate optical power of +7dBm in-fibre is injected into the circuit. Fig. 4a shows the static performance of the circuit when 160Gb/s signals are routed through a two-stage path. The performance is assessed with bit error rate measurements showing a power penalty of 0.8dB. Fig. 4b shows that the data integrity is maintained on all the multiplexed channels while maintaining error free operation at -19.5dBm. Error free operation has also been achieved when routing through the maximum four stages with a different multiplexing scheme [4].

Dynamic routing is studied by addressing the crossbar electrodes with fast pulse generators. The optical state transition time is measured to be 1.2ns. Electrode *j* is biased at the low state and electrodes *g* and *h* are reconfigured during the measurements. Fig. 5 shows one tributary of the dynamically routed 160Gb/s signal. The upper time-traces highlight the switching response when only one path is selected at a time. A complete suppression of the signal is achieved with the electrodes in the off state. The bottom time-trace shows the time aggregated channels from the two paths.

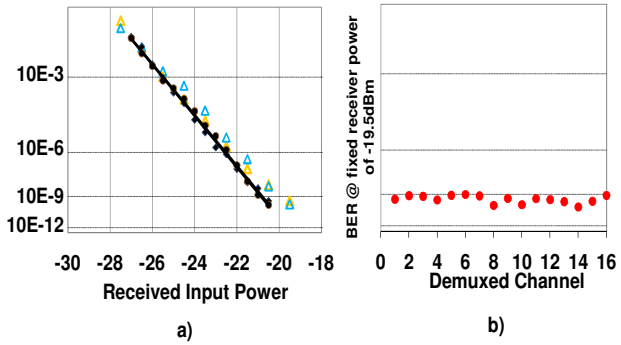


Fig. 4. a) Bit Error Rate performance showing for clarity two out of sixteen demultiplexed channels. b). Error performance at receiver power -19.5dBm for all sixteen demultiplexed tributrary channels.

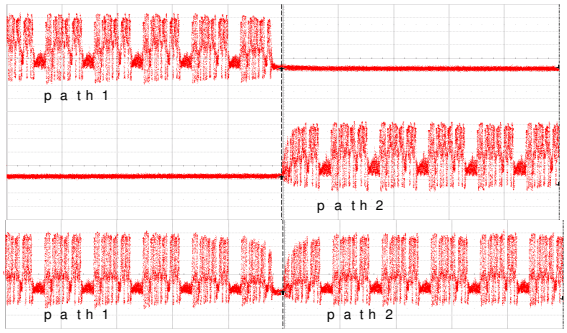


Fig. 5. Dynamic routing of a OTDM 160Gb/s input signal. (73ns timebase)

IV. Conclusion

The first monolithic multistage interconnection network using active passive integration is presented. A high extinction ratio, good optical signal to noise ratio, low loss and fast nanosecond rise time are all exhibited within the same circuit. The presented architecture is intrinsically scalable to higher network connections. The record 160Gb/s line-rate highlights a highly promising route to high-capacity and large scale photonic circuit integration.

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