Wafer Bonding and Heterogeneous Integration: III-V/Silicon Photonics

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Abstract. *The use of bonding technology to integrate III-V opto-electronic components on top of a silicon-on-insulator (SOI) integrated waveguide circuit is presented. III-V laser diodes and photodetectors fabricated on and coupled to an underlying SOI waveguide circuit are considered.*

Introduction

Photonic integrated circuits (PICs) offer the potential of realizing low-cost and compact optical functions. Silicon-on-insulator (SOI) is an emerging material platform for this integration, due to the large omni-directional refractive index contrast that can be achieved. Moreover, the massive CMOS processing infrastructure can be used to process these optical components. The integration of light emitters, optical amplifiers and detectors operating at telecommunication wavelengths is hampered by the indirect band gap of silicon. Although several advances are being made to achieve light emission from silicon, either by changing the silicon material on a nano-scale or by exploiting its non-linear optical properties, in the foreseeable future these devices will not outperform their III-V semiconductor counterparts, supplying state-of-the-art optoelectronic components for the telecommunication market nowadays. In order to create photonic integrated circuits comprising both active and passive optical components, the heterogeneous integration of passive silicon-on-insulator waveguide circuits and active InP/InGaAsP components is proposed. To decrease the cost of the integration process, both in time and consumption of expensive III-V material, a die-to-wafer bonding process is proposed in this paper, in which unprocessed InP/InGaAsP dies are bonded, epitaxial layers down, to the processed silicon-on-insulator wafer. This reduces the material consumption, as III-V semiconductors are only bonded where they are needed, and reduces the time to perform the integration process, as limited alignment accuracy is needed due to the absence of structure on the epitaxial layers. After removal of the InP substrate, active opto-electronic components can be fabricated in the InP/InGaAsP epitaxial layers, using wafer-scale processing, while being lithographically aligned to the underlying SOI features. The fabrication process is outlined in figure 1(a). In this paper we will outline the technology we developed for integrating the InP/InGaAsP epitaxial layer structures on a silicon-on-insulator material platform using adhesive DVS-BCB die-to-wafer bonding. While there are various methods to create an InP/InGaAsP epitaxial layer structure onto the SOI waveguide wafer (hetero-epitaxial growth, molecular bonding, adhesive bonding, anodic bonding, metallic bonding), adhesive bonding offers some significant advantages over other bonding methods. The relaxed requirements on surface cleanliness, contamination and surface roughness combined with the planarizing action of the adhesive spin coating

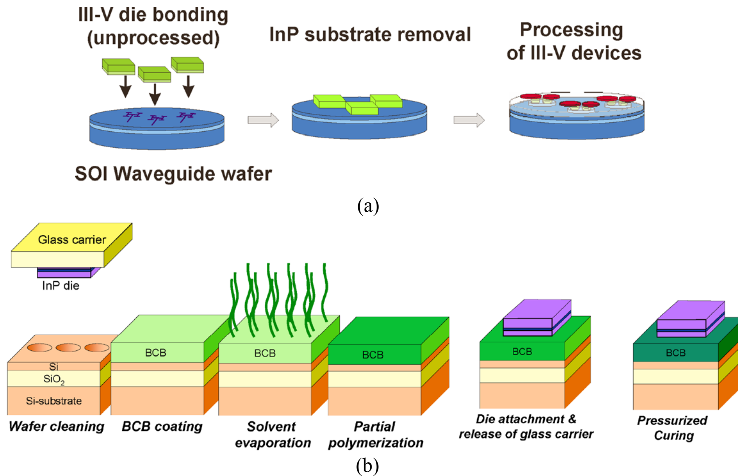


Figure 1: III-V/Silicon photonics integration (a) and the process flow for DVS-BCB bonding (b).

process, offer a significant reduction in surface preparation. Moreover, the integration process is a low temperature process, reducing the stress in the bonded stack due to the difference in thermal expansion coefficients between silicon and III-V semiconductor. The thermosetting polymer DVS-BCB (divinylsiloxane-bis-benzocyclobutene) was selected for process development due to its excellent planarizing properties, its high glass transition temperature (supplying sufficient postprocessing thermal budget), its low shrinkage and the fact that no byproducts are created upon cure. After integration of the InP/InGaAsP epitaxial layer structures, a myriad of optical components can be fabricated on the III-V/Silicon photonic integrated circuit. In this paper we report on the successful fabrication of integrated laser diodes and on the fabrication of integrated InP/InGaAsP photodetectors, both coupled to the underlying SOI waveguide circuit.

DVS-BCB die-to-wafer bonding technology

The DVS-BCB bonding process is outlined in figure 1b [1]. The cleaning of both the III-V die surface (which is temporary attached to a glass carrier) and the SOI wafer surface was optimized in order to remove pinned particles from the bonding interface. On the SOI wafer surface, a Standard Clean 1 solution ($1NH_3{:}4H_2O_2{:}20H_2O$ at 70C) is used to lift off particles. On the III-V die, the removal of a sacrificial InP/InGaAs layer pair using $3HCl{:}H_2O$ and $1H_2SO_4{:}3H_2O_2{:}1H_2O$ respectively, resulted in particle and contamination free surfaces. The DVS-BCB layer is spin-coated afterwards onto the SOI waveguide circuit and is pre-cured in order to evaporate the solvents. After the pre-cure, the III-V die is attached to the SOI and released from the glass carrier, and the III-V/SOI stack is cured at 250C. Temporary attachment to a glass carrier allows easy handling of small III-V dies and paves the way to multiple die-to-wafer bonding, as multiple III-V dies can be attached to a single carrier, ultimately populating a full 200mm SOI wafer using a single cleaning and bonding step. After bonding, the InP growth substrate is removed using a combination of mechanical grinding and chemical etching using HCl, until an etch stop layer is reached. Three different SEM cross-sections of III-V/SOI substrates are shown in figure 2, illustrating the range of bonding layer thickness that can be achieved. This wide range of thicknesses can be achieved by diluting commercial DVS-BCB solutions using mesitylene.

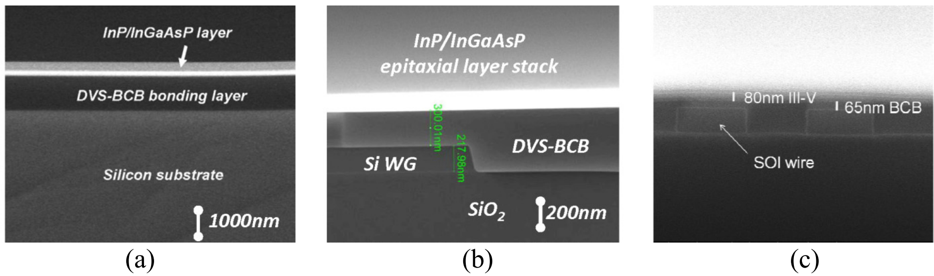


Figure 2: SEM cross-section of DVS-BCB bonded III-V/Silicon substrates showing a variety of bonding layer thicknesses that can be achieved: micrometer-range (a), sub-micron range (b) and 100nm range (c).

Heterogeneously integrated laser diodes on SOI waveguide circuits

Based on this technology, laser diodes were heterogeneously integrated on the SOI waveguide circuit. We proposed the concept of using an electrically injected III-V microdisk laser to generate light on the silicon platform. Although the demonstrated electrically injected devices were based on molecular die-to-wafer bonding [2], a DVS-BCB bonded microdisk laser is also feasible. DVS-BCB bonding has the additional advantage of a better control of the bonding layer thickness (ultimately defining the coupling between the III-V laser and the SOI waveguide) compared to molecular bonding, as in the latter case the bonding layer thickness is determined by a blind CMP polishing step of the SiO_2 covering the SOI waveguide circuit. Currently, continuous wave optically pumped DVS-BCB bonded microdisk lasers coupled the underlying SOI waveguide circuit have been demonstrated, as shown in figure 3a. 1µW of optical power is coupled to the SOI waveguide, for a 260nm DVS-BCB layer. Fabrication of electrically pumped devices is ongoing. A schematic of the microdisk structure is shown in figure 3b.

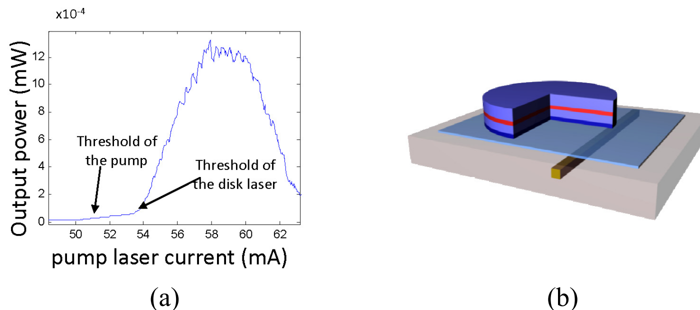
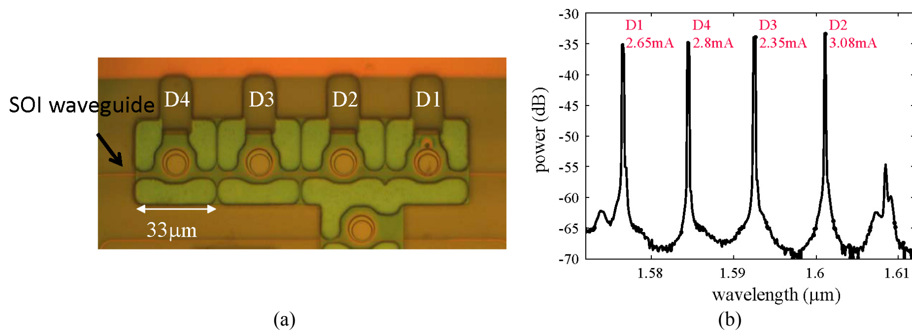


Figure 3: optical power coupled to an SOI bus waveguide in a continuous wave optically pumped DVS-BCB bonded microdisk laser (a) and schematic of the characterized device (b)

Besides single microdisk lasers, a multi-wavelength laser structure was fabricated as shown in figure 4a (before microdisk metallization). By slightly changing the radius of the microdisks coupled to a single SOI bus waveguide, the emission wavelength of the individual microdisks is varied. In figure 4b, the spectrum of the light coupled to the SOI bus waveguide is plotted, showing the four laser wavelengths equally distributed over the free spectral range of the disks. In order to achieve a uniform optical output power over the different channels, the drive current needs to be individually modified.

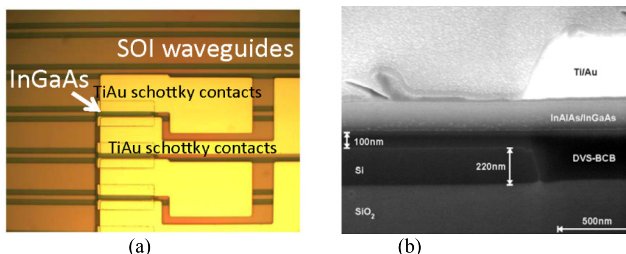


(a) (b)

Figure 4: Optical microscope image of a cascade of four rings coupled a single SOI bus waveguide (a) and the obtained optical spectrum in the SOI waveguide mode (b)

Heterogeneously integrated photodetectors on SOI waveguide circuits

Besides laser diodes, also metal-semiconductor-metal photodetector (MSM) using an InGaAs absorption layer were realized, as shown in figure 5a. The coupling between the SOI waveguide and the photodetector is achieved by vertical directional coupling between the SOI waveguide and the lossy III-V waveguide mode confined by the lateral TiAu contacts. The 3µm spacing between the coplanar Schottky contacts equals the SOI waveguide width. The dark current of the device was 3.0nA at a bias voltage of 5V (for a device length of 25µm), while the detector responsivity is 1.0A/W at 1.55µm and a bias voltage of 5V. A cross-section of the device is shown in figure 5b [3]. Currently the integration of these photodetectors on top of functional SOI waveguide circuits is ongoing and will be presented at the conference.



(a) (b)

Figure 5: Top view of the fabricated III-V metal-semiconductor-metal photodetectors integrated on an SOI waveguide platform (a) and a cross-section of the device (b).

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