Hybrid Integration for Advanced Photonic Devices

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Abstract. *Hybrid photonic integration with passive assembly techniques allows compact optical modules to be realised with high optical performance and low packaging cost. Recent advances in integrating semiconductor optical amplifiers into practical all-optical signal processing circuits is described, with advanced applications from optical memory to sophisticated burst-mode optical regenerators.*

Introduction

The ability to easily combine different optical components via photonic integration is widely recognised as one of the key strategic technologies for the future. Within photonics, it is also acknowledged that using one material system for monolithic integration is not always viable for all the required optical functions. In addition, the optical performance of monolithically integrated devices is often compromised to some degree and this has been a barrier to commercial realisation of devices. In other words, compactness on its own is not sufficient for practical use of integrated devices – optical performance is also vitally important. To address this, CIP has pioneered a photonic integration approach using hybrid integration technology that allows different high-performance optical components (active and passive) to be combined into integrated modules [1]. This is achieved by using precision design and fabrication techniques that allow the different component piece parts (as shown in Figure 1) to be simply pushed together via passive assembly. We believe that this approach not only offers the necessary precision for low-loss coupling of single-mode optical components, but will also lead to greater module scalability, flexibility and lower cost manufacturing in the future.

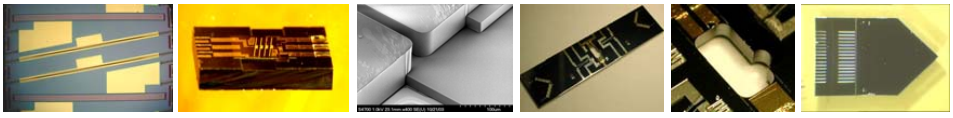


Figure 1: Photographs of the hybrid integration platform piece parts (L to R: precision cleaved semiconductor optical amplifier (SOA) monolithic twin chip, Si daughterboard, polymer precision edge stops, PLC, recess in PLC for SOAs, fibre ribbon clip).

In this paper, recent advances in the passive assembly hybrid integration platform are described. In particular, its use in combining InP actives (SOAs) and passive devices (optical isolator) with planar silica waveguides to create advanced optical signal processing circuits is demonstrated. These modules use the nonlinear optical properties of SOAs to allow one light beam to be switched with another [2]. SOAs are attractive components because they are compact (~mm size), can be electrically powered, provide optical gain and require very low switching energies (<100fJ). To operate at high switching speeds (>40Gb/s), the SOAs typically have to be incorporated into a compact optical interferometer, such as a Mach-Zehnder device, in order to exploit the cross-phase as well as the cross-gain dynamics of the optical switching. These types of

integrated interferometric devices are well suited to hybrid integration of the active SOAs with low-loss, passive planar silica waveguide interferometers. The planar silica waveguides allow other optical functions, such as wavelength selective combiners/splitters, to also be included in the module [3] and provides a scalable path to compact arrays of 40Gb/s regenerator devices.

Hybrid Integration Platform

CIP has been developing a hybrid integration platform over many years that is based on passive assembly for low cost. The basic principle of this platform is that the active and passive devices are designed together so that the complete integrated circuit is optimised, rather than just the individual components. For example, the active InP chips (e.g. SOAs) are designed with optical mode expansion and mechanical precision cleave features that make the overall chip size larger, but allows the chip to be passively aligned to the planar lightwave circuit (PLC). The PLC ($\Delta \sim 0.75\%$) also has some mode expansion to minimise coupling loss and retains the attractive silica waveguide features of low transmission loss (<0.1dB/cm) and high thermal stability. The active chips are aligned to the PLC by mounting the chip on a silicon submount (or 'daughterboard') and then mounting the assembled daughterboard onto the PLC (or 'motherboard') so that the active InP components fit into precision machined or etched holes in the motherboard, as schematically shown in Figure 2. The lateral position of the daughterboard is defined by precision polymer (SU-8) stops that are lithographically defined on the motherboard. Vertical position is defined by the height of the silica cladding above the silica waveguides in the PLC. These processes can give micron scale alignment accuracy which is sufficient to align single-mode optical elements with <1dB in coupling loss.

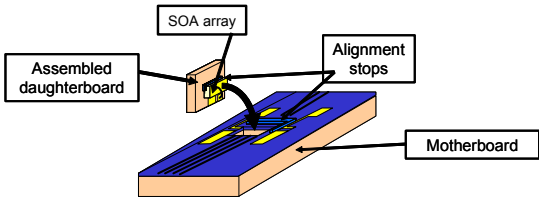


Figure 1: Schematic diagram of the CIP hybrid integration platform with passive assembly.

Active Devices

One of the advantages of the hybrid integration approach is that the active InP devices used in the platform can be optimized without regard to epitaxial or processing compatibility with the other optical parts of the integrated circuit. Hence, we use advanced InP multiple quantum well (MQW) SOA devices in a buried heterostructure device geometry since these offer very high performance [4] and are manufacturable. These SOAs achieve state-of-the-art performance by also incorporating optical mode expanders, tilted facets and coatings to reduce the residual facet reflectivity to $<10^{-5}$ and hence maintain high optical gain (>30dB) at high injection currents. This performance is vital to achieve the very fast gain recovery lifetimes required for high-speed optical processing modules [5]. These SOAs can be produced in monolithically integrated,

precision cleaved arrays, as shown in figure 3, for one-step assembly into hybrid integrated devices.

Figure 3: Photograph of monolithic SOA chips (single, twin, quad and octo).

Passive Devices

The PLC is used in the integration platform to interconnect the relevant active devices with waveguide structures such as interferometers and couplers. A typical PLC is shown in figure 4, which comprises 4 parallel Mach-Zehnder interferometers, Y-branch combiners, thermo-optic heaters and a parallel (12 way) fibre clip connection on each end. The 2 holes in the PLC are to accommodate the assembly of two monolithic quad arrays of SOA devices.

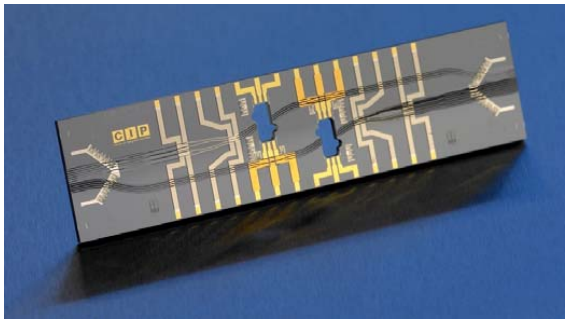


Figure 4: Photograph of a 4 channel SOA-MZI motherboard PLC.

In addition to waveguide devices, other passive optical element can be designed to fit with the hybrid platform. Figure 5 shows an example of a passively assembled optical isolator that uses the same assembly approach to provide on-chip isolation for the optical circuits.

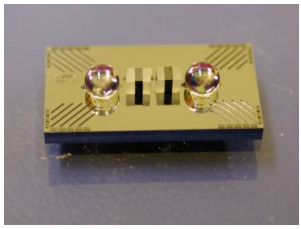
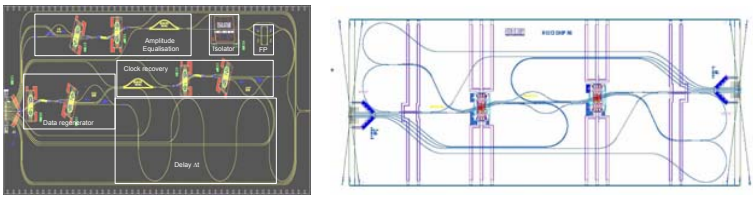


Figure 5: Photograph of a passively assembled optical isolator for the hybrid integration platform.

Hybrid Integrated Optical Circuits

By combining the functionality of the various active and passive components of the hybrid integration platform, it is relatively easy to form advanced optical circuits. Two different designs are shown in figure 6 for a 40Gb/s time-of-flight optical memory and a 40Gb/s burst-mode receiver (BMR) [6]. Each circuits uses common optical piece parts, with only the waveguide circuitry differing to define the interconnections and hence the circuit functionality.



(a) *(b)*

Figure 6: Waveguide design layouts for (a) 40Gb/s BMR and (b) optical memory.

The fabricated BMR circuit and package is shown in figure 7, and comprises 9 different assemblies of SOA arrays, fibre arrays, optical isolator and a Fabry-Perot filter.

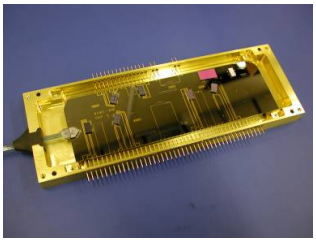


Figure 7: Photograph of the fabricated 40Gb/s BMR circuit.

Up-to-date results on these circuits and other details of the hybrid integration platform will be given during the conference presentation.

References

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